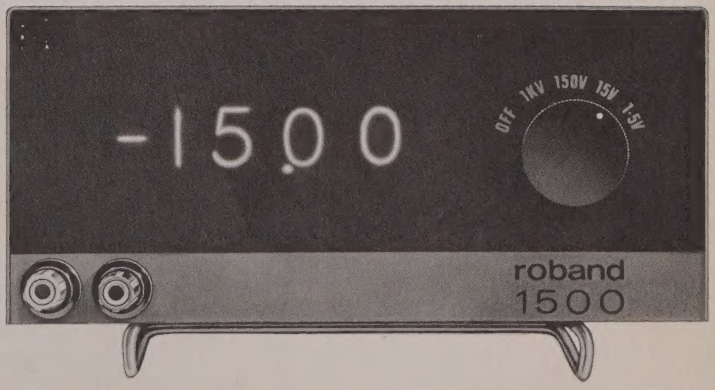
# roband manual

## 1500 DIGITAL VOLTMETER



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*The company reserve the right to amend the specification of this equipment or to supply units that may vary in detail from the description contained in this publication.*

## 1. SPECIFICATION

The Roband 1500 is a compact, four range (1mV to 1000V) digital voltmeter with automatic sign change. It is simple to operate, very reliable, and is therefore suitable for use both as a bench instrument and in a wide range of low cost, digital indication and analogue – digital conversion applications.

**SPECIFICATION:**

**Ranges:**

| | Range | Sensitivity | Input Resistance | Offset Current |
|---|---|---|---|---|
| 1. | ± 1.500V DC | 1mV | > 100M ohms | $10^{-10}$A |
| 2. | ± 15.00V DC | 10mV | > 10M ohms | |
| 3. | ± 150.0V DC | 100mV | > 10M ohms | |
| 4. | ± 1000V DC | 1V | > 10M ohms | |

**Range Selection:** Manual, with automatic positioning of decimal point.

**Polarity:** Automatic, with minus sign display.

**Accuracy:** (all ranges) 0.2% of reading, ± 1 digit (for ± 20% nominal mains variation and +10°C to +40°C ambient range.

**Zero Stability:** No zero adjustment is necessary.

**Long Term Stability:** 0.1% per annum, first year: 0.02% p.a. typically, subsequent years. All ranges internally adjustable.

**Series Mode Rejection:** 27 dB at 50Hz
Increasing 20dB per decade.

**Common Mode Rejection:** (10K unbalance)
DC : 120 db
AC : 80 db at 50Hz,

**Common Mode Voltage:** (DC plus AC peak)
1000V maximum relative to earth

**Over-voltage:** 1000V maximum, all ranges,
Reading limits automatically at 1500.

**Filter Response Time to Step Input:** (for full accuracy) 1 sec.
A correct reading is given by the first sample AFTER 1 second has elapsed from the instant of step input.

**Sample Rate:** 2 per sec. nominal

**Power Input:** 115/230V RMS ± 20%, 40-60 Hz.
15VA

**Operating Temp. Range:** 0°C to 50°C

**Storage Temp. Range:** −10°C to + 70°C

**Dimensions:** Width : 19 cm (7.5"), Panel Height: 8.6 cm (3.4")
Depth : 22.6 cm (8.9")
Weight : 2.6 Kgs (5¾lbs)

**Tilt Stand:** Readily removable to facilitate mounting unit into standard rack.

**Front Panel Appointments:** 2 input terminals (4mm socket types) at 19mm centres. Rotary switch, 5 way including Mains ON/OFF position.

**Rear Panel Facilities:** Optional Extra: 50 way socket, carrying external readout connections for decimal readout only.

**External Readouts:**

**Outputs:** Minus, 1000, 3 decades of decimal output.

Levels: ON (1) nominally –4V at 5mA max.
OFF (0) between +60V and +140V at 50microA max.

**Control Input :** Hold

Levels: Hold reading: –6V nominal at 2mA
Normal running: OV, or open circuit.

External readouts can provide direct drive for external neon indicators. Connections to external logic circuits must incorporate blocking diodes to prevent current drain from the positive OFF level. Details of suitable interface circuits may be obtained from Roband Electronics Limited

**NOTE** The signal input is not isolated from the external readouts. Therefore, when external circuits are connected to the external readouts both the overall common mode rejection and maximum common mode voltage will be reduced, due to the external circuits.

In particular, the external circuits associated with the voltmeter external readouts must be isolated from the signal circuits.

## 2. OPERATION

### 2.1 Mains Supply

Units are normally supplied connected and fused for operation from a mains supply in the range 185–275 volts RMS.

If the unit is to be used from a mains supply in the range 93–132 volts, the transformer primary links, and the fuse rating, must be altered. See Section 3.2 for details.

**Mains Supply Connections**

These should be made to a three-pin plug, or other suitable terminals.

Red lead is connected to Line
Black lead is connected to Neutral
Green lead is connected to Earth.

CAUTION The Earth connection MUST be made, to ensure that the case of the instrument is safely earthed.

### 2.2 Normal Use

Switch on the instrument and select the appropriate range, by means of the range switch.

There are no external controls for adjustment of zero or of calibration.

The Display reads to 1500 full scale.
A negative sign is illuminated for negative signal input, absence of this sign indicates positive input.
Illuminated decimal points indicate the range in use.

### 2.3 Overvoltage

Indicated by a reading of 1500.
The unit is undamaged by application of up to 1000V, on any range. (It is advisable to remove signal before operating the range switch, if the overvoltage is greater than 300 volts).

CAUTION The unit should always be switched off by means of the range selection/on/off switch, (which isolates the signal input terminals) since the overvoltage protection circuits only function when the unit is operating.

### 2.4 Ripple Rejection

Errors in readings can result from the presence of ripple (A.C.) on the D.C. signal. A fixed filter in the voltmeter input circuit attenuates ripple by a factor of approximately 30 at 50Hz, and by a proportionally greater amount at higher frequencies. Thus, input ripple of 60mV pk to pk at 50Hz can give a reading error of 1mV.

Sampling is locked to mains frequency in order to eliminate jitter on the display due to ripple at mains frequency and harmonics.

**Sample Rate and Response Time**

The presence of the input filter produces a lag in response to a step input. This is not more than 1 second, for a step input change from minus to plus full scale. A correct measurement occurs at the first sample after 1 second has elapsed from the time of signal step.

The sample rate is nominally twice per second.

### 2.5 Common Mode Characteristics (measurement of small difference signal at a high voltage relative to earth).

Either terminal may be raised to 1000 volts (D.C. plus peak AC) relative to earth (chassis).

Reading errors due to a common mode input are proportional to the magnitude of common mode signal, and to the impedance between the common mode signal and the signal low terminal (black) of the voltmeter.

D.C. common mode rejection is better than 120db with 10K ohm source impedance, i.e. 1000 volts common mode signal can give a maximum error of 1mVolt with 10K source resistance.

A.C. common mode rejection is typically 80db with a 10K ohm resistance to signal low i.e. 1mVolt reading error results from 10 volts R.M.S. at 50Hz (typically).

### 2.6 Application Notes

**External Scaling**

Inputs may be scaled externally to give readings on the 1.5 volt range in engineering units.

The source impedance of an external attenuator should not exceed 200Kohm (or 1M ohm with a corresponding increase of the input step response time to 2 seconds.).

Precision metal film or wirewound resistors should be used, with provision for adjustment of scaling.

**External Readouts**

A list of functions, with operating voltages and currents, is given in the specification. Details of interface circuits suitable for use with external logic may be obtained from Roband Electronics Limited.

**NOTE** When external circuits are connected to the external readouts, the combined system has a reduced common mode rejection. The maximum common mode voltage may also be reduced.

**CAUTION**

The signal input circuits must be isolated from circuits associated with external readouts. Failure to observe this precaution may result in damage to the instrument.

**Use of "Hold" Signal** (available on units with External Readout)

Application of a negative "Hold" signal prevents further sampling for the duration of this signal.

A delay of 5 millisec should be allowed after the application of a "Hold" signal, before using the digital output signals. This allows time for completion of digitisation which may be in progress at the instant of applying the "hold" signal.

**NOTE*** The first sample after removal of a "hold" signal may give an incorrect reading. The second and subsequent samples will be correct.

**Conditions of Use for Maximum reliability**

The unit is designed for reliable operation to stated accuracy over the temperature range $10^{o}C$ to $40^{o}C$.

Reliability and accuracy improve as the operating temperature range is restricted, operation at temperatures close to $20^{o}C$ being ideal.

The ventilation slots, (base and rear) must not be obstructed.

Reliability is worsened by shock, vibration, corrosive atmosphere, high relative humidity.

Reliability may be worsened by long periods of storage without use, particularly in hot or damp conditions. To minimise such deterioration, operation for a period of 6 to 8 hours every three months, is recommended.

The mains supply must not exceed 20% above nominal value, i.e. 276 volts R.M.S. or 138 volts R.M.S.

Care should be taken to avoid short circuits between lines, when external connections are made to the instrument via the optional rear connector.
In particular, *the signal input must be isolated from other external circuits connected to the voltmeter.*

## 3. CIRCUIT OPERATION

The principle employed is voltage to time conversion, using the step-ramp technique.

A capacitor is charged to the signal voltage. Polarity is sensed, and a reference current of the appropriate polarity is switched to discharge the capacitor linearly to 0 volts. During this discharge time, clock pulses are counted to provide an indication of signal voltage.

The reference current is then disconnected, and the signal voltage is switched to recharge the capacitor. This cycle is repeated nominally twice per second.

### 3.1 General Description (Refer to Block Diagram Fig. 1).

Consider a signal voltage applied to the input terminals on the 1.5 volt range.

The signal is filtered to reduce errors in reading due to ripple on the input by R 38, R 39 (Power Supply Board) and C1 (analogue board). The voltage across C1 causes C5 to charge through R25, R27.

Extremely small variations of voltage at the input of amplifier A1 are sufficient to cause large output changes, therefore the input of amplifier A1 remains very close to 0 volts. Thus as C5 charges, A1 output (signal low) moves from 0 volts to a voltage equal to the signal input, while the signal high terminal falls to 0 volts.

At an instant determined by the logic, the SIGNAL SWITCH closes to 0 volts, preventing flow of signal current through R27. Simultaneously, R14 is connected to the appropriate reference voltage, passing a constant current to discharge C5, linearly.

As A1 output passes through 0 volts, the output of the zero detector, A2, changes state, resetting the logic. The signal and reference switches open, allowing the signal to recharge C5, as before.

The above sequence of signal and reference switching is controlled by the logic in the following manner.

A mains frequency square wave, produced on the power supply board, combines with trigger timing circuits to produce a trigger pulse. This pulse sets a "sample" bistable, which opens the clock pulse gate. Clock pulses at 1MHz are then fed to the three decade counters, which count up from the previously displayed number, passing through 999, 000 and continuing.

As the counter moves from 999 to 000, the "carry 500" signal changes state, setting the polarity selection circuits. These cause the signal switch to close, and R14 to be connected to either a positive or negative reference voltage, determined by the output of A2,the zero detector.

C5 discharges linearly towards 0 volts. As A1 output passes through zero, A2 output changes state, resetting the sample bistable, also the polarity selection circuits. Counting ceases, and the original input conditions are restored.

Because the discharge of capacitor C5 is essentially linear, the time taken to discharge from the signal voltage to zero is proportional to signal voltage. The rate of discharge is adjusted so that the number of clock pulses appearing in this time is numerically equal to the applied voltage.

The state of the counter at the end of count is decoded into decimal form, and displayed on neon number indicator tubes. Negative input signal polarity is indicated, positive input signals produce no polarity display. A count greater than 1000 causes the $\div 2$ bistable to set, driving the 1,000 display.

Further trigger pulses are inhibited by the trigger timing circuits for nominally 500m sec. During this time the measured value is displayed, and capacitor C5 again charges to the signal voltage.

Signals higher than 1.5 volts are attenuated by R 29, 30, 32, 34, 36, 37 to give ranges of 15 volts, 150 volts and 1,500 volts. full scale. The maximum signal voltage is limited to 1,000 volts, however. Decimal point displays are controlled by the position of the range switch.

## 3.2 Power Supply

### Mains Transformer

The primary may be linked for 230V (nominal) or 115V (nominal) operation.

See Fig. 2 for details of link positions. Notice that a single link provides 230V operation, 2 links are required for 115 volt operation. A fuse rated at 150mA is required for 230V operation.

A fuse rated at 250mA is required for 115V operation.

The instrument will operate from any supply voltage within ± 20% of the nominal setting.

NOTE Operation at voltages more than 20% lower than nominal will cause inaccurate readings. Operation at more than 20% above nominal may damage the instrument.

The transformer is double screened. The primary screen is connected to mains earth. The secondary screen is connected to the signal low terminal. The two screens are isolated to give minimum capacitive and resistive coupling between voltmeter circuits and earth.

### D.C. rails

**+300V Unstabilised at 10mA (referred to –6 volt stabilised)**

This rail is used to supply the neon indicator tubes, and consists of MR1 and C1, in a simple half wave rectifier circuit. Ripple across C1 is approximately 15-25 volts depending upon load. A maximum additional current of 20mA may be drawn for external display etc.

**+12Volts Stabilised at 25mA**

MR3 and C2 provide a halfwave rectified supply. The ripple voltage across C2 should be approximately 1½ volts.

The circuit VT2, VT3, VT4 and associated components form a conventional regulator circuit.

Variations of output voltage, due to load or input variations, appear on VT3 emitter through zener diode MR6. Approximately half of the output variation also appears at VT3 base, due to the potential divider. The difference causes a change of current from VT3, in phase with the supply output variation. This change is amplified and inverted by VT4 and R3. Thus the output at VT2 emitter is stabilised. C4 and R4 ensure high frequency stability.

**Stabilisation Ratio and Output Impedance**

Stabilisation against variations of the 300 volt rail is approximately 75,000 to 1. Maximum variation with mains supply of the 300V rail (± 60 volts) corresponds to approximately ± 1mVolt output variation. Output resistance is approximately 50m ohms. Temperature coefficient is better than 0.02%°C.

**Output Ripple**

Typically 300 micro volts peak to peak.

**Adjustment**

The 12 volt rail may be adjusted by RV1, to 12 volts ± 20mVolts

**Excess Current Capability**

14mA max. at 20% high mains voltage) at 50°C ambient
28mA max. at 10% high mains voltage.

**–6 volt Stabilised at 150mA**

This stabilised rail is combined with the positive and negative reference rails.

MR4, 5 and C3 provide a full wave rectified supply. Ripple voltage across C3 is approximately 1V.

A temperature compensated reference zener diode MR8, is "suspended" between the 12 volt and –6 volt rails by R15 and R18. The zener voltage is centre tapped by two precision resistors, R16 and R17. The stabiliser circuit VT6, 5 and 7, maintains this centre point virtually at 0 volts by varying the –6V rail.

The 6 volt rail is made up from the sum of the negative reference and a voltage equal to (12volts – V ref positive) X R18/R15.

The stability and regulation of the 6 volt rail is sufficient not to degrade the performance of the reference rails due to the shift of VT6b base. High frequency stability is obtained by C5, R14, C7 and C9.

**Stabilisation Ratio and Output Resistance**

Stabilisation against mains supply variations is approximately 4000 to 1.

Output resistance is approximately 25m ohm.

**Temperature Coefficient**

The two reference rails remain balanced to typically 1mV, and the absolute value to 0.1% in 10°C.

**Linearity Correction**

For a variety of reasons, the voltage/time relationship of the voltage/time conversion circuits of the voltmeter is not truly linear, when a fixed reference voltage is used. To correct this, a small signal, proportional to the input signal voltage, is added to the reference.

The output of A1 (block diagram), designated signal low, is attenuated by R10, R11, on the power supply board, and fed to VT6a base. The stabiliser circuit, acting as an operational amplifier, balances this signal by a similar signal on VT6b base, and thus also on the reference rails.

It will be seen that the –6 volt rail must also move with these signals. The variation is only a few millivolts, and does not affect unit operation.

**Output Ripple**

50 Hz and 100Hz ripple are typically less than 1m Volt peak to peak. Ripple due to linearity correction reaches approx. 10mV pk to pk at maximum signal inputs.

In addition, there is a high frequency ripple of approximately 1mV pk to pk at about 2MHz, emanating from the clock pulse generator. This ripple is minimised by the use of a 0.1 microfarad decoupling capacitor on the control logic board.

**Adjustment**

None provided. With the + 12 volt rail correctly adjusted, the –6 volt rail will be within 4% of its nominal value.

**Excess Current Capability**

20mA at 20% high mains, 60mA at 10% high mains, 50°C ambient.

**50Hz Square Wave**

The voltmeter triggering is locked to the mains supply frequency to minimise noise on readings when the signal input contains significant ripple at mains frequency and its harmonics. A mains supply frequency square wave is produced on the power supply board by feeding VT1 base with 225Vr.m.s. through R2. Diode MR2 limits negative excursion of VT1 base.

The square wave at VT1 collector, is also used to switch the modulator and demodulator transistors of the drift correction circuit employed on the analogue board.

## 3.3 Logic Circuits

These comprise 3 boards each containing a decimal counter, with associated decimal decoding, number tube drive circuits, and neon display tubes; and one other board containing miscellaneous logic circuits. These boards are described in detail below, and their function in the overall instrument operation is detailed in section 3.1 (General Description).

**Basic Circuits**

The following basic circuits are used many times.

The circuit of Fig. 4.1 performs a NAND (not and) function. When all inputs A and B (and C) are positive (1) the output is NOT positive (0). An unconnected input is effectively positive.

Conversely, if any input A or B or C is NOT positive (0) the output is positive (1).
Thus a gate with only one input used becomes a simple inverter.

Two gate types are used, FCH191 contains four gates in one package, each with two inputs. This is generally known as a 4 x 2 input gate, or a quad 2 input gate. FCH171 contains three gates, each with three inputs. This is a 3 x 3 input gate, or a triple 3 input gate.

In the accompanying circuits, gates are shown as in Fig. 4.2

When considering the more complex logic circuits, it is not necessary to consider the circuit of each individual gate. It is sufficient to remember the simple logic rules:-

all inputs positive – output negative
any input negative – output positive

One output can, in general, drive up to 7 inputs.

**Gate Delays**

There is a delay in output response to input change, of a few nanoseconds, typically 20-30n.secs. It is sometimes important to take note of this.

**"Wired Or" Connection Fig. 4.3**

This term is used to describe the connection together of two outputs.

If A and B are positive (1) or if C and D are positive (1) the combined output is negative.

**Bistable Connection Fig. 4.4**

Assume A = 0, B = 1.

Then Q = 1, $\overline{Q}$ = 0

If A now changes to 1, the circuit remains in this stable state. It will change state if B moves to 0. $\overline{Q}$ then becomes 1, and Q becomes 0. B can now be restored to 1, and the circuit will remain in this second stable state.

Thus the bistable can be caused to switch from one state to the other by a brief pulse on the appropriate input.

Notice that, once set, (Q=1), the circuit is impervious to level changes at A, it will respond only to a negative signal on B. The converse is also true.

Notice also, that if A remains at 0, negative pulses on B will cause positive pulses to appear at $\overline{Q}$ but the bistable will not change state.

This bistable may also be controlled by a WIRED or connection to one output (Fig. 4.5)

If A = 0, B or C = 0, then $\overline{Q}$ = 1, Q = 0

A can now change to 1, and Q, $\overline{Q}$ maintain their states.

If B and C = 1, $\overline{Q}$ = 0 and Q = 1 regardless of the state of A. In this case, pulses appearing on A will not only fail to switch the bistable, while B and C = 1, these pulses will not disturb the outputs Q and $\overline{Q}$ at all.

**Capacitor, Resistor, Diode, Gate – Fig. 4.6**

This circuit is frequently encountered in discrete component logic. In this case, the diode is actually one input of a DTL gate, only the capacitor and resistor are shown on circuit diagram.

Square waves fed into A are differentiated, producing positive and negative pulses at C. The diode blocks positive pulses and passes negative pulses only when B is negative. When B is positive, the negative pulses are blocked.

## 3.4 Control Logic

**Clock Pulse Generator**

VT1, VT2, VT8 and associated components: This is a simple multivibrator, temperature compensated by VT8, R24, R25, R.26.

**Trigger Timing Circuits (waveforms Fig. 5.1)**

Comprising VT5, VT6, VT7, part of IC5, and associated components. Initially, assume VT7 conducting, VT6 off. Thus IC5 pin 8 is positive.

50 Hz square waves, from the power supply board, are passed through VT5 stage to produce a square wave output of approximately 3 volts amplitude, with fast edges. This signal enters two C, R, diode gates, C7, R18 and C8, R19 and 23, which are biassed by IC5 pin 8 not to pass pulses.

At some arbitrary time, VT6 conducts switching off VT7. This releases the input on pin 6 of IC5.

If VT5 output is already negative, or when it next moves negative, the bistable sets, enabling the two CRdiode gates. VT5 output moves positive, in response to the mains frequency input, then again negative. Thus, up to this point, there is a minimum period of nominally 10m sec. during which C9 charges through R22 and VT6 base.

At this point (the negative transition of VT5 collector) the pulse from C7 resets the 1000 bistable (part of IC4) and sets the sample bistable (A, Figs. 5.1, 5.2).

The pulse from C8 fires monostable VT6, 7 via MR1. The monostable inhibits further triggering for nominally 500m sec.

The voltmeter is now triggered to digitise and the trigger timing circuit has reverted to its initial conditions (A, Fig. 5.2)

Note, the trigger circuit may be held by the application of a negative level to pin 5 of IC5 (–6V at approximately 2mA.)

**Digitisation (waveforms Fig. 5.2)**

Initially, the V ref + bistable, V ref – bistable (IC1) and signal switch bistable (part of IC2) are reset, that is, IC1 pins 1, 4, and IC2 pin 8, are positive.

(A. Fig. 5.2) The 1000 bistable is reset (IC4 pin 1 positive), and the sample bistable is set (IC3 pin 2 positive). The clock pulse gate inverts the clock signals into IC4 pin 9, to produce count pulses on pin 4 (IC4).

The three decade counter counts up, and as it passes from 999 to 000, the 500 signal moves negative (B. Fig. 5.2).

The 1000 bistable is unaffected, because of the positive level through R2.

Either V ref + bistable or V ref – bistable is set by the pulse through C1, depending on the state of the zero detector output. Notice that the reference bistable which remains reset, produces no unwanted pulse on its V ref switch output.

The signal switch bistable is also set by the pulse through C1.

Thus, the signal and reference switches are closed, causing the discharge of a capacitor from signal potential towards zero, as previously described.

The CR diode gate utilising C1, R1, is inhibited, the gate comprising C2, R2 is enabled. Should a further negative transition occur on "500" (occurring at the transition 999-1000) the V ref bistables are unaffected and the 1000 bistable is set (C. Fig. 5.2)

When the signal switch bistable became set, the level on IC3 pin 8 changed from negative to positive. At approximately the same time, one of pins, 9, 10, changed from positive to negative due to the setting of one of the V ref bistables.

IC3 pin 8 is fed through an inverter from IC2 pin 8, with a total of 3 gate delays from the 500 pulse out of C1. IC3 pin 9 or 10 moves negative after 2 gate delays from the same pulse. This ensures that during the transition of inputs of this gate, at least one input is always negative, and IC3 pin 6 remains positive.

When the output of amplifier A1 passes through zero, the zero detector changes state, resetting the V ref bistable that was previously set. Pins 8, 9 and 10 of IC3 are now all positive, pin 6 moves negative, applying a reset to the sample bistable (D. Fig. 5.2).

The sample bistable is interlocked with the count line, to ensure full width pulses and thus prevent miscounting which could occur with partial pulses. When the count line moves positive, or if it is already positive, the sample bistable resets in response to the output of IC3 pin 6. This closes the clock pulse gate (the output of which remains positive) and also applies a reset to the signal switch bistable, IC2 pin 6. Because of this, the level into IC3 pin 8 moves negative, removing the reset level to the sample bistable. (Again there is sufficient delay in the loop to ensure that the sample bistable is reset before the reset input is removed). (Fig. 5.3).

Counting has now ceased, the V ref switches and signal switch are open. Digitisation is complete.

**Overrange**

When "500" is positive, each positive "count" edge produces a negative output from IC4 pin 8. The CR diode gate utilising C3 R3 will block these pulses between 500 and 999, but will pass the pulse at 1500. This pulse, occurring while "count" is positive, resets the sample bistable, and thus the signal switch bistable. Counting ceases.

**Polarity Store**

This bistable is slaved to the polarity of reference used in the previous digitisation. Either pin 3 or pin 13 IC2 is negative during digitisation, setting the bistable to the appropriate state. IC2 pin 1, when positive, drives VT3 to illuminate ILP1, the negative polarity indicator.

**1000 display**

When the 1000 bistable is set, IC4 pin 11 is positive, driving VT4 to illuminate ILP3, the 1000 display.

Neon ILP2 acts as a catching diode protecting VT3 and 4 against overvoltage when their respective lamps are not in use.

## 3.5 Counter

The counter consists of a divide by 5 section followed by a divide by 2 stage.

The first section uses three bistables, with C R diode gates connected to give a "twisted ring" configuration, and with an input to bistable A from C.

Consider bistable B inputs (waveforms Fig. 8.1). When A is reset (A negative, $\overline{A}$ positive), the count pulses through C4 are blocked, the first pulse through C1 will reset B. Conversely, if A is set, the first clock pulse will set B.

In a similar way, C will follow B.

When C is set, A will reset on the next pulse, but when C resets, A is set immediately, by the direct connection to IC1 pin 13.

Therefore, the counter will follow this sequence.

$A\,\overline{B}\,\overline{C}$
$A\,B\,\overline{C}$
$A\,B\,C$
$\overline{A}\,B\,C$
$\overline{A}\,\overline{B}\,C$
$A\,\overline{B}\,\overline{C}$

Notice that, $\overline{A}\ \overline{B}\ \overline{C}$ is impossible

$\overline{A}\ B\ \overline{C}$ is impossible

$A\ \overline{B}\ C$ leads to $A\ B\ \overline{C}$ in one count. The three unused binary states are either inhibited, or resolved within one count after switch on.

Bistable D changes state every time bistable C resets, and generates a symmetrical square wave carried to the count input of the next decade.

The complete counter sequence is shown diagramatically in Fig. 8.2

**Decode and Number Tube drive**

The full counter sequence is

| | | | | | |
|---|---|---|---|---|---|
| 0 | = | $A\,\underline{\overline{B}}\,\overline{C}\,\overline{D}$ | 5 | = | $A\,\overline{B}\,\overline{C}\,D$ |
| 1 | = | $A\,\underline{B\,\overline{C}}\,\overline{D}$ | 6 | = | $A\,B\,\overline{C}\,D$ |
| 2 | = | $\underline{A}\,B\,\underline{C}\,\overline{D}$ | 7 | = | $A\,B\,C\,D$ |
| 3 | = | $\underline{\overline{A}\,B}\,C\,\overline{D}$ | 8 | = | $\overline{A}\,B\,C\,D$ |
| 4 | = | $\overline{A}\,\underline{\overline{B}\,C}\,\overline{D}$ | 9 | = | $\underline{\overline{A}\,\overline{B}\,C\,D}$ |
| | | | | | $A\,\overline{B}\,\overline{C}\,\overline{D}$ |

Notice first, that each combination of A, B, C, occurring in the numbers 0-4 reoccurs in the numbers 5-9. The state of bistable D defines which of two numbers in each case.

Consequently, the emitters of VT1, 3, 5, 7, 9, (the transistors driving numbers 0-4) are connected to D, which is negative for 0-4 and positive for 5-9. The series diode MR6 introduces a level shift to ensure correct biassing of non-conducting transistors. Similarly, emitters of VT2, 4, 6, 8, 10 (driving numbers 5-9), are connected to $\overline{D}$ through MR.7.

Secondly, it can be seen that each of the five states of the divide by five counter is fully defined by only two bistable states (underlined above). For example, the combination A $\overline{B}$ occurs only at count 0 and (5). If and only if, A and $\overline{B}$ are both positive, either VT1 or VT2 will conduct, depending on the state of D, to illuminate either 0 or 5.

Similar reasoning applies to each of the other four pairs of numbers.

**Neon Number Tube**

One of ten cathodes is caused to conduct by conduction of one of the ten transistors VT1-10. Neon current is limited by R16.

Each tube contains two decimal point cathodes, one to the left and one to the right of the number. In all three decades, the left hand decimal point is used, selected by range switch position. These provide indication of 1.5V, 15V and 150V range. 1000V indication is provided by selection of the right hand decimal point of the units tube.

## 3.6 Analogue Circuit

The general principles of operation have been covered in Section 3.1

**Amplifier A1**

This consists of IC1, IC3, VT9, 10, 11, 12, 14, 15 and associated components.

**Main Amplifier Section**

VT10 and 11, field effect transistors used as source followers, buffer the inputs (pins 2 and 3) of ICI. To ensure that the DC input requirements of IC1, (μ A 702C) are met pin 1, normally 0 volts, is fed from emitter follower VT12, which in turn is fed from VT11 source. Thus pin 1 is maintained about half a volt more positive than pins 2 and 3.

Capacitor C8 provides a low source impedance to VT12 base at high frequencies, and serves to decouple pins 1 and 3 of IC1 from high frequency transients.

Diode MR1 ensures that under overload conditions, pin 2 cannot move significantly positive of pin 3, preventing "latch up" of IC1.

Amplifier A1 is subjected to 100% feedback at high frequencies, through C5, and is stabilised by C9 and R42, giving a unity gain bandwidth of about 10MHz.

**Drift Correction**

VT10 gate acts as the "virtual earth" input to amplifier A1. This point is maintained close to 0 volts, and at a stable voltage which is practically independant of variations of temperature or of power supplies, by a drift correction circuit. This circuit employs IC3, transistors VT9, 14, 15 and associated components. The DC potential of VT10 gate is coupled through R28 and R31 to VT9 emitter. When VT9 is switched off, this potential appears on C12. If VT9 is switched on, its emitter moves to a potential of typically less than 1mVolt negative of 0 volts. This potential is very stable with temperature.

VT9 is switched on and off by a 50Hz square wave, generated on the power supply board, and coupled through R30 and MR4. C12 is fed with a square wave alternating between VT10 gate potential and the "on" voltage of VT9. This square wave is buffered by field effect transistor VT14, and a.c. coupled into IC3 input through C14. The square wave is amplified by a factor of 2,000 or more, in IC3.

When VT9 conducts, VT15 also conducts, as their bases are driven by the same 50Hz waveform. During the "conducting" half cycle, C17 charges to the output voltage of IC3, through R50 and VT15. During the "non-conducting" half cycle, IC3 output changes by an amount proportional to its input square wave, (which in turn is proportional to the DC error between VT10 gate and VT9 "on" voltage). This change is coupled through C17. Thus at VT15 emitter there is a square wave from nominally 0 volts to a potential proportional to the DC error on VT10 gate, and of opposite polarity (since IC3 inverts the square wave).

The square wave at VT15 emitter is averaged by R33 and C7, to provide a DC level which biasses VT11 gate.

At equilibrium, VT10 gate potential is close to −1mvolt. VT11 gate is at such a potential as to maintain a balanced output. Variations of a few millivolts at VT11, due to temperature effects, etc., are provided by variations of a few microvolts at VT10. The major variation at VT10 gate is caused by change with temperature of VT9 "on" voltage. This is typically less than 100 microvolts over the working temperature range of the voltmeter.

IC3 gain is reduced at high frequencies by C16. DC bias is provided by R48, 49, decoupled by C14. MR5 prevents an excessive positive input to pin 2.

The switching waveform at VT9 base is coupled by transistor internal capacitance onto VT9 emitter, producing alternate positive and negative spikes. Capacitor C6 filters these spikes, preventing their appearance at the amplifier input. A small mean current is produced by those spikes. This current combines with leakage currents from VT1, 3, 6, 7, 8 and 10 to produce an offset current at the input. This current is balanced by a current produced in R44 by a small voltage from RV7.

**Overload Protection**

It is essential that the voltmeter input circuits should withstand a substantial overvoltage without damage. It is desirable that such protection should be accomplished without disturbing the equilibrium of the drift correction circuit, which would take many seconds to recover from such a disturbance.

The bases of transistors VT4 and 5 are biassed to, nominally + 2 volts and – 2 volts respectively. If the input voltage exceeds approximately 2.5 volts, IC1 output conducts into VT4 or 5 emitter, clamping signal low at 2.5 volts. The current passes through one of the diode connected transistors VT6, 7 and causes a voltage drop across R25, R28, R29 (1.5 volt range). Sufficient current passes to just drop the excess input voltage across these resistors.

**Zero Detector**

A1 output is connected to IC2 pin 2 through R36. Diodes MR2 and 3 limit the input voltage. IC2 is used as a high gain comparator, the output switching VT13 which in turn drives DTL gates on the control logic board. RV6, R38, 39, 37 provide adjustment for the total offset voltages of the system, being adjusted to give zero reading for zero input. The function of C13, R54, is discussed below under "Timing".

**Signal and Reference Switching**

VT8 is switched on for the duration of digitisation by the signal switch level from the control logic board. When switched on, VT8 emitter moves to a voltage of approximately – 1mvolt, this voltage being relatively stable with time and temperature.

The positive reference is switched by VT3 (normally non-conducting). R16, 17 ensure a small positive bias on VT3 base when "+V ref switch" is at 0 volts. The transistor conducts when "+V ref switch" is at –6 volts. Again, the collector-emitter "on" voltage is about 1mvolt, and relatively stable. The negative reference is similarly switched by VT1. VT2 is diode connected in series with VT1 base, to reduce leakage current.

**Scaling**

The magnitude of the discharge current into C5 governs the scaling on the 1.5 volt range, since this controls the rate of discharge of C5. R12 and R15, selected on test, provide coarse adjustment for negative and positive references respectively, while RV4 and RV5 provide fine adjustment.

A simple attenuator, R29, 30, 32, 34, 36, 37 provides x 10, x 100 and x 1000 attenuation, with fine adjustments for each range.

Resistors R31, R33, R35 pad the attenuator source resistance viewed from C1, to give a filter time constant virtually unaffected by range setting. (The attenuator components are fitted on the power supply board, adjacent to the range switch).

**Timing**

Errors in timing, related to the clock frequency, can cause significant non-linearity near zero.

Ideally, the discharge of C5 should commence half a clock cycle before the clock pulse which steps the counter from 0 to 1. This assumes instantaneous switching of reference current, and no lag in the integrator, zero detector, and control logic.

In practice, the logic initiates C5 discharge at the negative transition of the 500 waveform, as the counter moves from 999 to 000. This waveform in fact lags about 300 n.sec (approx. .3 digit) on the 999-000 clock edge. There are further small lags in the control logic, the integrator, and the zero detector, and a lag together with an effective ramp rise of the switched reference. In total, these lags exceed .5 digit.

The lags may be compensated by a single phase advance resistor, R24. Variation of this value affects the point of "break" from one number to the next at readings of a few digits. However, the imperfect switched reference waveform leads to some non-linearity at readings from 0-5 digits. To compensate this, an additional network (R36, R37, C13) is incorporated at the zero detector input, giving a second phase advance due to R54.

**NOTE** The signal low terminal must **NEVER** be connected to the 0 volt rail.

## 4. MAINTENANCE

### 4.1 Routine Maintenance

At 6 months, 1 year, and annually thereafter, check; Current zero, voltage zero, and calibration on all ranges.

Checks should be performed at a room temperature of 20° to 25°C after not less than 2 hours running with the cover in position. After completing checks, the cover may be removed, and adjustments made, if necessary. Replace the cover, and recheck after a further 30 minutes. Note Adjustments should be made in the order stated.

#### 4.1.1. Current Zero

Select 1.5 volt range, with input terminals open circuit. Allow reading to settle. RECORD READING.

Adjustment of current zero control is necessary if the steady reading exceeds 4mVolts (Accessible through screen of analogue board).

#### 4.1.2 Voltage Zero

Select 150volt range.
Apply a variable signal of approximately +1 volt, and adjust this input signal until the reading of the Roband 1500 varies between 010 and 011.

Measure the applied signal to a resolution of 5 millivolts and note value.

Reverse the input signal, and note the value of input required to produce a reading varying between −010 and −011.

The two measured values should be equal ± 15mvolt. Adjust volts zero control if necessary (Accessible through screen of analogue board).

RECORD READ

NOTE The point at which readings "break" between adjacent numbers is very sharply defined. Calibration and zero adjustments can therefore be made to an accuracy of a fraction of a digit, by varying the applied signal to locate the point of "break", and adjusting the instrument so that this point is optimal.

#### 4.1.3 Calibration

Select 1.5 volt range.

Apply a variable signal of approximately +1.5 volts, and adjust this input signal to obtain a reading varying between 1.499 and 1.500. The input signal value should be 1.4995 ± 0.0005 volts. Adjust Positive Cal. control if necessary (Accessible through screen of analogue board).

RECORD INPUT

Repeat with a negative input signal, adjusting Negative Cal. control if necessary (Accessible through screen of analogue board).

#### 4.1.4 Select 15 volt Range

Apply a variable signal of approximately 15 volts, and adjust this input signal to obtain a reading varying between 14.99 and 15.00. The input signal value should be 14.995 ± 0.005 volts, Adjust 15 volt range control if necessary (accessible through switch).

#### 4.1.5 Select 150 volt Range

RECORD INPUT

Apply a variable signal of approximately 150 volts, and adjust this input signal to obtain a reading varying between 149.9 and 150.0. The input signal value should be 149.95 ± 0.05 volts. Adjust 150 volt Range control if necessary (Accessible through switch).

RECORD INPUT

#### 4.1.6 Select 1000 volt Range

Apply a variable signal of approximately 1000 volts, and adjust this input signal to obtain a reading varying between 999 and 1,000. The input signal value should be 999.5 ± 0.5 volts.
Adjust 1000 volt range control if necessary.

RECORD INPUT

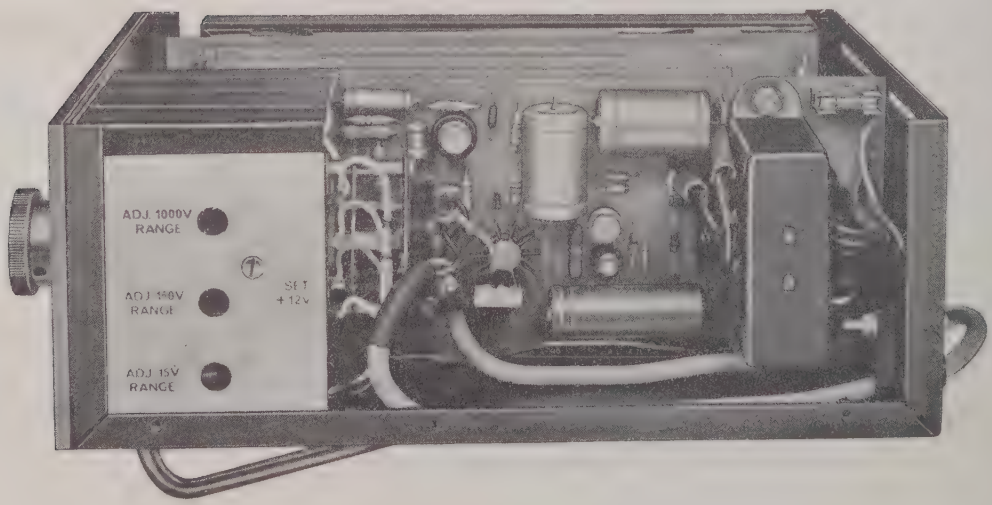
NOTE The screen fitted to the range switch may be removed, if required, to facilitate adjustment of 15 volt, 150 volt and 1000 volt ranges. It must then be replaced.
Avoid contact with switch terminals, some of which carry high voltages.

CHECK OVERLOAD OPERATION

CHECK − DC INDICATION

END

VOLTS
CURRENT
ZERO
−CAL
+CAL


ADJ. 1000V
RANGE
ADJ. 150V
RANGE
ADJ. 15V
RANGE
SET
+12v

### 4.2 Full Setting-Up Procedure

To be used if Power Supply Board, Analogue Board or Control Logic board is changed.

#### 4.2.1 Before Switching On after changing Power Supply Board.

Check that the transformer primary links, and fuse rating, are correct for the mains supply to be used. (See Sect. 3.2)

#### 4.2.2 Before Switching On, after changing Analogue Board.

Check that resistors or shorting links are fitted in positions R12, R15, R24, analogue board (Replace screen before continuing checks).

#### 4.2.3 Power Supply Checks

Monitor +12 volt rail relative to 0 volts.
Connect signal input terminals together.
Switch on.

Adjust +12 volt rail to +12.00 volts, $\pm$ .02 volts (RV1 power supply board).

Check –6 volt rail: – 6 volts $\pm$ .25 volts. (relative to 0 volts).

Check +300 volt (relative to –6volts): +305 volts $\pm$ 60 volts.

Check $\pm$ 3.1 volt reference rails (relative to 0 volts): 3.1V $\pm$ .16V
These rails should be equal to within 60m Volt.

Monitor 50Hz Square Wave output: square wave of approximately 12 volts pk-pk.

NOTE It is convenient to use individual sockets which fit the power supply output pins. A.MP type 163088-2 have been found suitable. These sockets should be insulated with suitable tape.

#### 4.2.4 Initial Zero Adjustment

Select 15 volt range
Adjust VOLTS ZERO (RV6, Analogue Board) to give zero reading.

Open circuit the input terminals, select 1.5 volt range. Adjust current zero to obtain zero reading. Allow sufficient time for readings to settle.

Connect input terminals together, and readjust volts zero control if necessary.

#### 4.2.5 Initial Calibration Adjustment

Selection of R12 and R15.

Select 1.5 volt range.

Apply a signal of approximately +1.4 volts, (known to an accuracy of 1m volt). Let the absolute value be V.

Rotate "positive cal" potentiometer fully clockwise. Note the reading given by the Roband 1500. Let this be R1.

Rotate "positive cal" potentiometer fully anticlockwise. Note the new reading R2.

Rotate "positive cal" potentiometer to a central position.

The value of resistor R12 requires to be changed by an amount given approximately by.

$$V - \frac{(R1 + R2)}{2} \times \frac{22}{R1-R2} \text{ K ohm}$$

or more simply, change of R12 is 2/3 of the number of digits error in reading at mid setting of positive cal control in K ohm R12 is increased to increase readings.

Apply a known negative signal of approx. – 1.4 volts (known to an accuracy of 1m volt).

Rotate "negative cal" potentiometer fully clockwise, then fully anticlockwise, noting the corresponding readings. Return potentiometer to a central position.

Calculate the change of resistance required of R15.

Disconnect the input signal, switch off. Remove outer screen from analogue board.

Locate R12, R15. Calculate the ideal value of each resistor by adding (or subtracting) the required change of value from the value already fitted.

Select a value for each resistor, from the E24 series*, to differ by not more than 5K ohm from the ideal value in each case. Fit resistors of the selected values in place of existing R12 and R15.

NOTE Resistors R12, R15 must be metal oxide resistors (Type TR5 or MR5 preferred) CARBON RESISTORS MUST NOT BE USED.

Replace screen. Switch on. Adjust positive and negative cal potentiometers to give approximately correct readings of positive and negative signals.

4.2.6 **Fine Zero Adjustment**

Select 150 volt range.

Apply a variable signal of approx. 1 volt, and adjust input until the reading of the Roband 1500 varies between adjacent numbers (e.g. 010, 011). Measure this signal to the nearest 5 millivolt and note value.

Reverse input signal. Adjust input to obtain "break" between the same two numbers. Note the value of the input signal required. Adjust "V zero" potentiometer so that these two readings are equal to $\pm$ 10mVolt.

4.2.7 **Selection of R24**

Ideally, readings will "break" between 10 and 11 for an input signal of 1.05 volts. If the required input signal differs from this by .02 volts or more, the value of R24 should be altered. Increase of the value of R24 increases the applied signal which is required to obtain the break, at the rate of approximately 10mV/33 ohm.

After replacing R24, the fine zero adjustment should be repeated if necessary.

**Calibration**

Select 1.5 volt range.

4.2.8 Apply a variable signal of approximately +1.5 volts, and adjust this input signal to obtain a reading varying between 1.499 and 1.500. The input signal value should be 1.4995 $\pm$ 0.0005 volts. Adjust Positive Cal. control if necessary (Accessible through screen of analogue board).

Repeat with a negative input signal, adjusting Negative Cal. control if necessary (Accessible through screen of analogue board).

4.2.9 **Select 15 volt Range**

Apply a variable signal of approximately 15 volts, and adjust this input signal to obtain a reading varying between 14.99 and 15.00. The input signal value should be 14.995 $\pm$ 0.005 volts. Adjust 15 volt range control if necessary (Accessible through switch).

4.2.10 **Select 150 volt Range**

Apply a variable signal of approximately 150 volts, and adjust this input signal to obtain a reading varying between 149.9 and 150.0. The input signal value should be 149.95 $\pm$ 0.05 volts. Adjust 150 volt Range control if necessary (Accessible through switch).

4.2.11 **Select 1000 volt Range**

Apply a variable signal of approximately 1000 volts, and adjust this input signal to obtain a reading varying between 999 and 1,000. The input signal value should be 999.5 $\pm$ 0.5 volts. Adjust 1000 volt range control if necessary.

NOTE The screen fitted to the range switch may be removed, if required, to facilitate adjustment of 15 volt, 150 volt and 1000 volt ranges. It must then be replaced.
Avoid contact with switch terminals some of which carry high voltages.

In addition to the adjustments described above, the following tests should be performed when the analogue board has been changed.

*E24 series.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91, 100.

**4.2.12 Input Overvoltage Protection**

To be checked in both polarities.
Select 1.5 volt range.
Apply a signal of approximately 10 volts.

Check that the reading limits at 1500.
Disconnect signal, and connect input terminals together.
(Use a break before make changeover switch).
Check that reading returns to zero within 4 samples.
Apply nominal 10V signal opposite polarity, repeat as above.
If these tests are satisfactory,
Repeat as above with signal of nominally 100 volts.
If satisfactory.
Repeat as above with the signal of nominally 1000 volts.
In this case, the signal will fall to a few millivolts within four samples, then decay slowly to zero. This is due to a secondary storage effect in the filter capacitor.

**4.2.13 Series Mode Ripple Rejection** 1.5 volt range.

Apply 1V R.M.S. 50Hz to the input.
Reading should not exceed 50mV.

**NOTE** 6.3V RMS 50Hz may be used for this test, to obtain a maximum reading of 315mV.

**4.3 Repairs**

It is recommended that faulty units be repaired by Roband Electronics Ltd. or their authorised agents.

Repairs may in general be made by replacing faulty printed circuit boards. Replacement boards are obtainable from Roband Electronics Ltd. or their agents. Note, however that replacement of certain boards necessitates complete recalibration of the instrument. (See Sec. 4.2).

**CAUTION! Use of soldering iron**

Soldering iron must be properly earthed, and the unit must be switched off and disconnected from external circuits, before a soldering iron is applied to the unit.

Sufficient voltage may be developed on the bit of an unearthed soldering iron, to destroy certain components of this unit.

**CAUTION! Use of oscilloscope**

When an oscilloscope is connected to this unit, the voltmeter signal inputs and external readout connections must be isolated from earth. Failure to observe this precaution will result in short circuits which will damage the unit. Low capacitance probes (less than 20 pf) should be used, when monitoring Logic and Analogue signals. Ensure probes are properly adjusted.

**4.3.1 Fault Diagnosis**

Faults may be located and rectified in most cases by substitution of boards. Some preliminary diagnosis is advisable, however, both to reduce the amount of substitution necessary, and to protect against damage of a substitute board by another fault in the unit.

**4.3.1.1**
**Power Supply**

Monitor the power supply rails, with 1000 volt range selected.

+12 volts $\pm$ 0.02 volts.
Load current typical: 25mA
Output ripple typical: 300microV pk-pk at mains frequency.

−6 volts $\pm$ 0.25 volts.
Load current typical: 140mA
Output Ripple typical: 1mV pk-pk at twice mains frequency together with 1mV pk-pk at 2MHz.

+300 volts (measured relative to −6 volt rail) +305 volts $\pm$ 60 volts.
Load current typical: 10mA
Output ripple typical: 20 volts pk-pk at mains frequency.

$\pm$ 3.1 volt reference rails 3.1 volts $\pm$ 0.16 volts.
These rails should be equal to within 60mVolt.

50Hz square wave:- Square wave of approximately 12 volts pk-pk at mains frequency.

Excessive output ripple, even at the correct D.C. voltage output, can indicate incorrect operation.

Incorrect operation may be caused by a fault outside the power supply board, which may in turn damage the power supply board.

If fault conditions indicate that this may be so, the outside fault must be rectified before fitting a replacement power supply board.

A power supply board which has been stressed in this way, may be independently tested, using the following dummy loads.

–6 volts to 0 volts 36 ohm, 3 watt wire wound
+12 volts to 0 volts 470 ohm, 1 watt, metal oxide film
+300 volts to –6 volts 30K ohm (5x1 watt, metal oxide film
150K ohm, in parallel).

4.3.1.2

**Counters**

Disconnect the "carry 500" signal between the hundreds counter and the control logic board.

With a dual trace oscilloscope in the "alternate" sweep mode monitor the clock input to the units counter board, and the "carry 5" output, using low capacitance probes (less than 20pf). Both traces should be triggered from the negative going edge of the "carry 5" signal.

Set the oscilloscope sweep speed to 1 microsec per division, and adjust the variable sweep speed to obtain one clock pulse per division.

Verify that the units counter is dividing by 10, with no jitter and no spikes on the "carry 5" signal.

Monitor "carry 5" and "carry 50" signals, triggering from "carry 50" with sweep speed set to 10 miscrosec. per division.

Verify correct operation of tens counter.

Monitor "carry 50" and "carry 500" signals, triggering from "carry 500" with sweep speed set to 100 microsec per division. Verify correct operation of hundreds counter.

Switch off unit, and reconnect "carry 500" signal.

4.3.1.3

**Display**

Display faults, such as inability to display certain numbers, superimposed blurred numbers etc. are usually readily traceable to the affected board.

4.3.1.4

**Detailed Diagnosis.**

More detailed diagnosis should be based on a knowledge of circuit operation. Attention is drawn to section 3, which describes circuit operation in detail.

### 4.3.2 Dismantling the Unit

1. Remove cover (4 screws)
2. Slacken mains cable securing clamp, and pass about 12 inches of cable into box.
3. Remove screen from Range Switch (1 screw)
4. Remove outer screen from analogue board (2 screws).
5. Remove knob from Range Switch (single grub screw) together with felt washer.
6. Using a box spanner, carefully unscrew the front panel fixing nut from the Range switch, and remove spring washer.
7. Gently ease range switch back through the front panel.
8. Release 50 way rear connector, if fitted (2 screws).
9. To release the bracket fixing the analogue board, place unit with rear left hand corner overhanging the edge of the bench. Hold the 4BA countersunk screw with a screwdriver beneath the base of the unit, while removing the nyloc nut.
10. Release power supply fixing bracket as in step 9.
11. Carefully lift the assembly out of the box, and place to the left side (terminal side).
12. The input lead may be disconnected from the input terminals if required, and the mains lead freed from the chassis.
13. Release clamping bar. Hold 4BA nyloc at power supply board with a spanner, while unscrewing 4BA nut at analogue board with a box spanner.
14. Remove clamping bar. The printed circuit boards may now be fanned out for ease of access. Care should be taken to adequately space and support the boards if power is to be applied, in order to prevent accidental short circuits.

### 4.3.3. Assembly of the Unit

1. Before assembly, carefully inspect the insulating tape on chassis lid, switch screen, and analogue screen box, for damage. Repair as necessary, using Scotch Tape No. 33.
2. Fit clamping bar, ensuring correct spacers are fitted in each position. ¾ inch spacers are fitted between power supply and units counter boards, and between each counter board. ½ inch spacers are fitted between hundred counter and control logic board, and between control logic and analogue boards.

   Ensure no wires are trapped while fitting clamping bar. Do not fully tighten.
3. Connect input lead to input terminals. The inner connects to the red terminal, the outer to the black terminal.
4. Enter mains lead through its clamp.
5. Place assembly into position in the box.
6. Fix Range Switch. Ensure that the printed circuit screen is properly located. Ensure that the spring washer beneath the fixing nut is not forced behind the perspex panel. Use box spanner to tighten nut, taking care not to damage perspex panel.
7. Pull mains lead through its clamp, leaving a small amount of slack within the box. Tighten mains lead clamp.
8. Fix analogue bracket and power supply bracket to chassis. Do not fully tighten.
9. Hold boards firmly in position, and tighten fixing nuts of power supply brackets, analogue bracket, and clamping bar, in that order.
10. Fix screens to analogue board and range switch.
    Check that all screens are well clear of the sides of the chassis.
11. Fit felt washer, and knob, to range switch.
12. Fit cover.
13. Check that the signal low (black) terminal is isolated from chassis (1000V megger). If it is not, remove the unit, examine the insulating tape for breaks and repair as necessary, with Scotch Tape No. 33. Check continuity from chassis to the mains earth input.

### 4.3.4 Removal of Individual Boards

It is possible, in most cases, to gain access to boards (for diagnosis etc), without dismantling the instrument.

**Analogue Board**

Remove outer screen to gain access to components. To release board, remove 4BA nut and washer on the clamping bar. Remove two 6BA hexagonal spacers. Release analogue board fixing bracket (rear of analogue board). The board can now be twisted carefully to allow unsoldering of leads, or changing of components. The box screen can be removed, to improve access.

Before replacing board, ensure nuts and lock nuts on the two 6BA screws fitted to the screen box are fully tightened.

NOTE There will be pick-up at mains frequency in the analogue circuit if the instrument is operated with the outer analogue screen removed. This will cause small errors in readings.

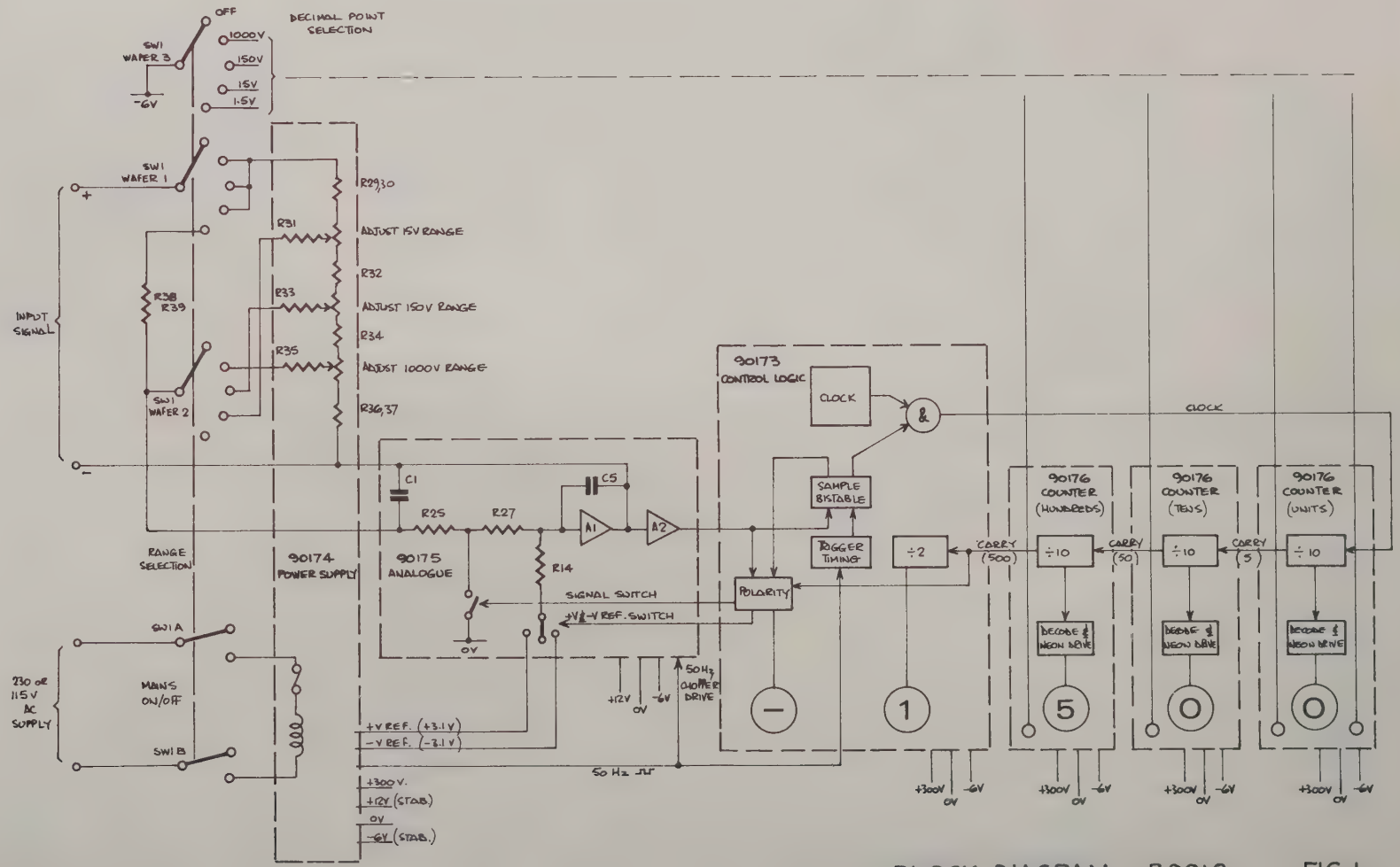
**Control Logic & Counter Boards**

Remove outer screen of analogue board, and the switch screen. Remove 4BA nut from clamping bar and withdraw clamping bar, while removing the spacers one at a time, until the board which is to be moved is free. Gently lift the front of the board until it clears the clamping bar, then replace the clamping bar, while refitting spacers. Replace analogue screen and switch screen. Ensure that the free board is positioned safely, with no possibility of accidental short circuit to other boards.

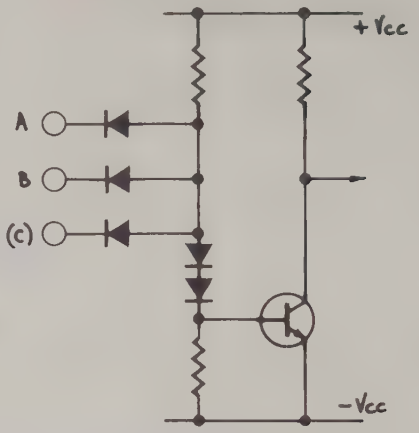
**Power Supply Board**

Most of the components on the power supply board are accessible to oscilloscope probes etc. Access to the copper track (for component replacement) is most easily obtained by removing the clamping bar, and moving clear the adjacent boards. If the board is to be changed, the connections at the front of the board may now be unsoldered also the mains supply connections.

Release the fixing bracket, and tilt board to allow the power supply outputs to be unsoldered. (There is one connection to these pins on the component side of the board).




BLOCK DIAGRAM B9218 FIG.1

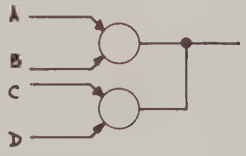



D.T.L GATE
FIG.4.1

SYMBOLS FIG.4.2

PART OF FCH91

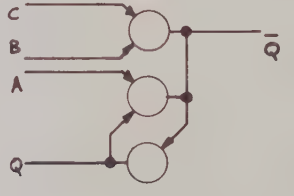
PART OF FCH91



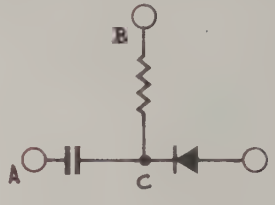

WIRED OR CONNECTION FIG.4.3

BISTABLE CONNECTION FIG.4.4

BISTABLE WITH WIRED OR FIG.4.5




CAPACITOR, RESISTOR, DIODE GATE FIG.4.6




BASIC LOGIC CIRCUITS B9221 FIG.4

FIG. 5.1. TRIGGER TIMING CIRCUIT WAVEFORMS

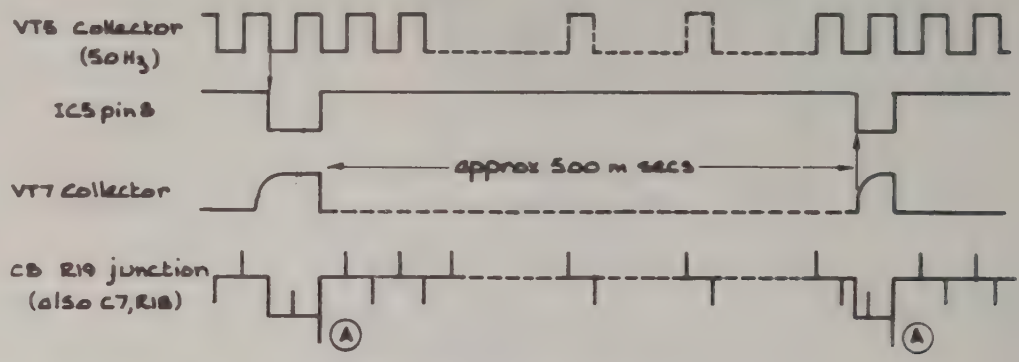



FIG. 6.2. WAVEFORMS DURING DIGITISATION
(Negative signal reading over 1000)

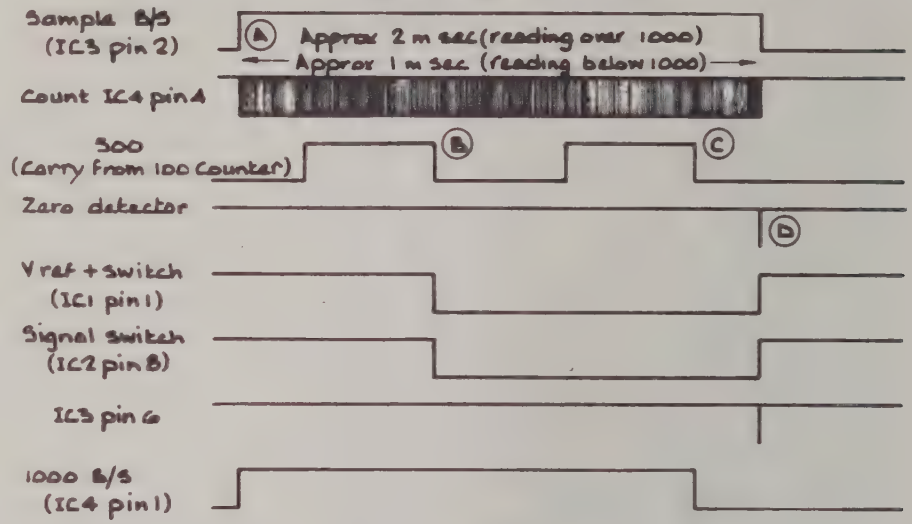
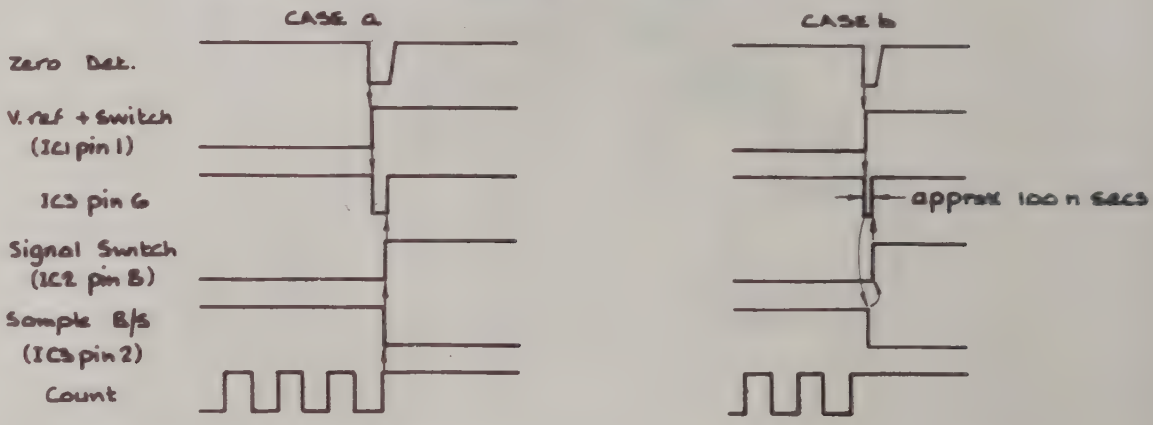
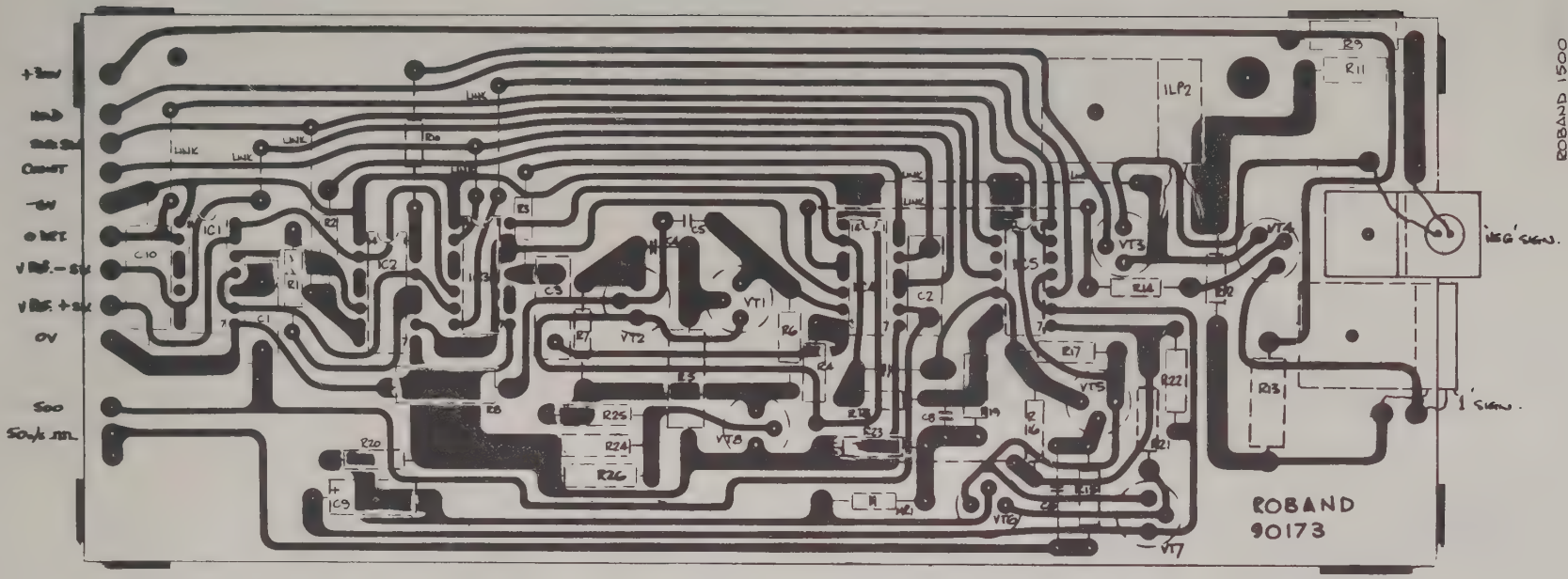


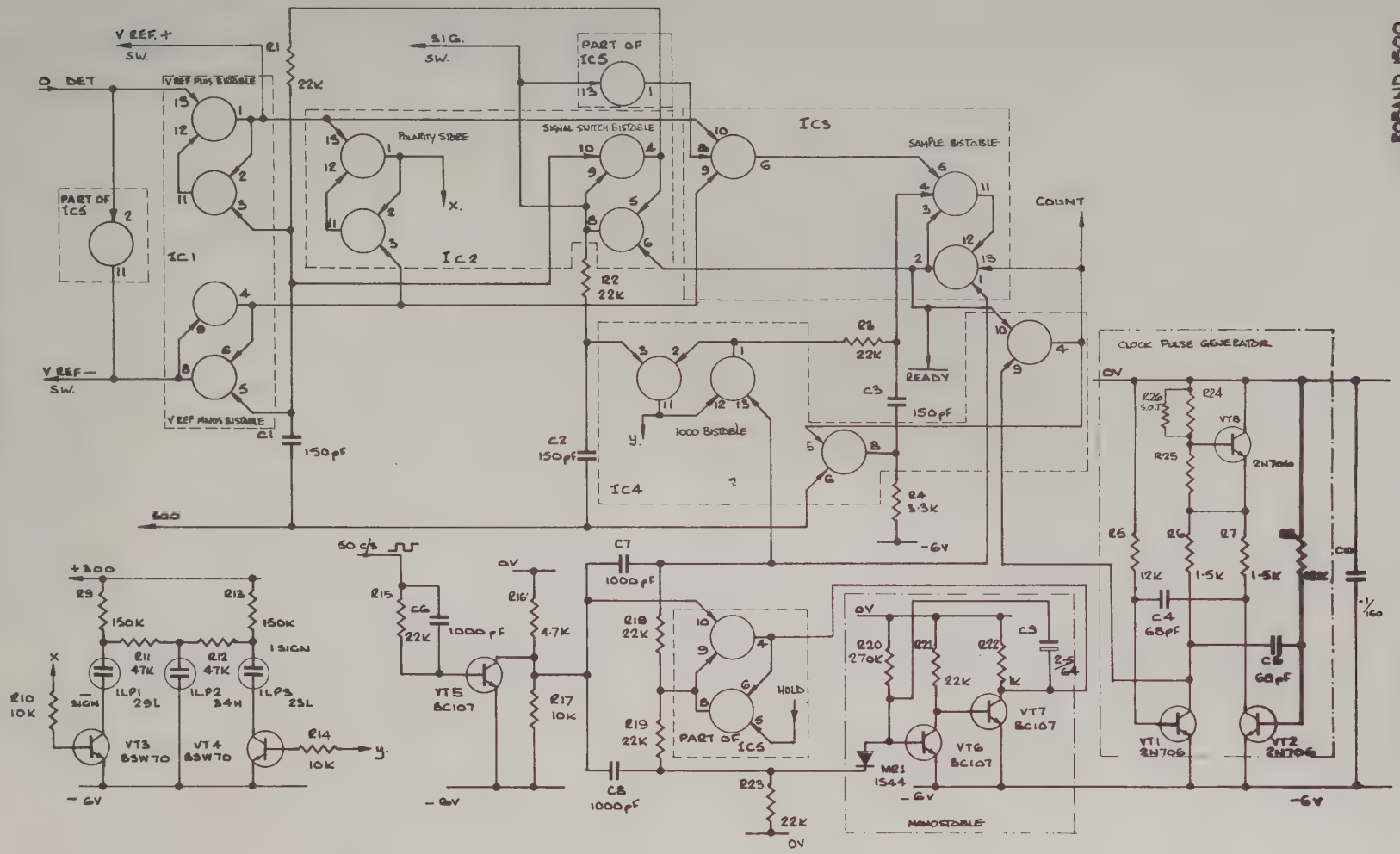

FIG 5.3. DETAIL OF END OF COUNT (FIG 5.2.D)




CONTROL LOGIC WAVEFORMS FIG.5 _B9222_

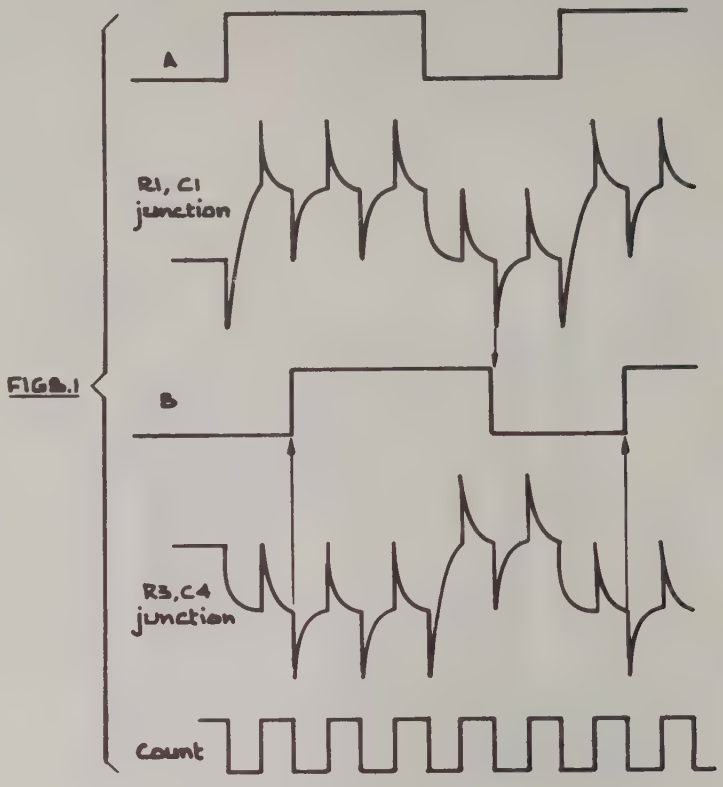



CONTROL LOGIC ASSEMBLY 90173 FIG. 6

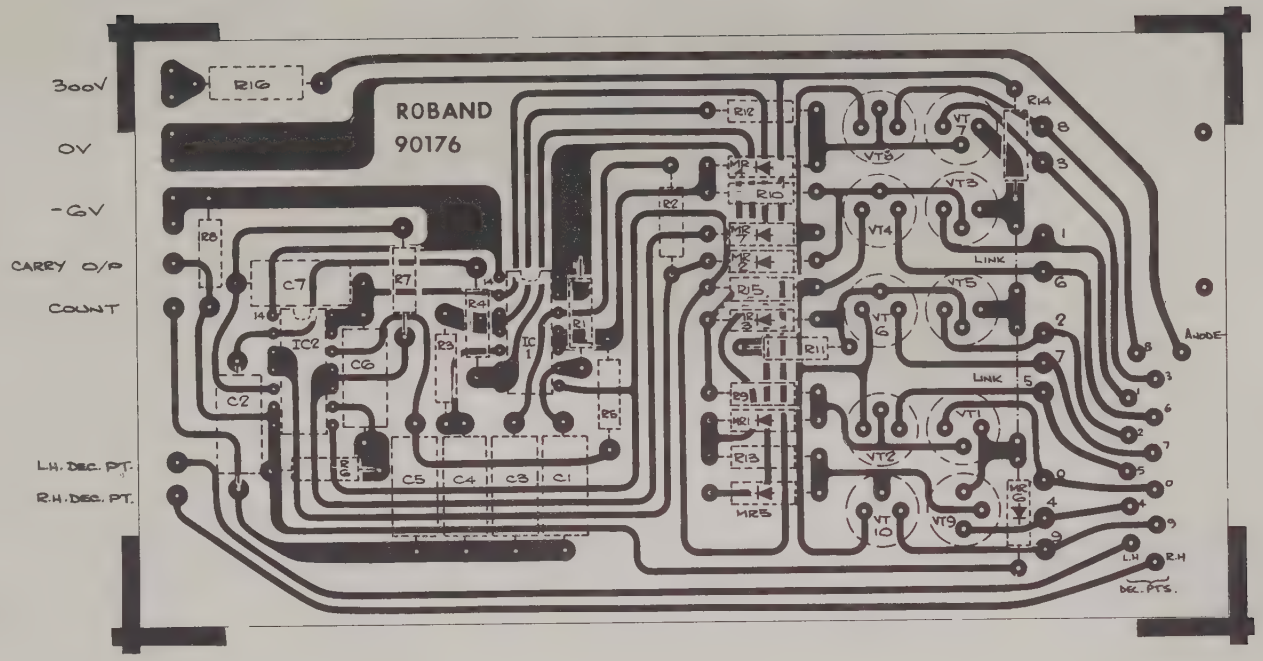



CONTROL LOGIC CCT. 901739 FIG.7

FIG 8 COUNTER WAVEFORMS

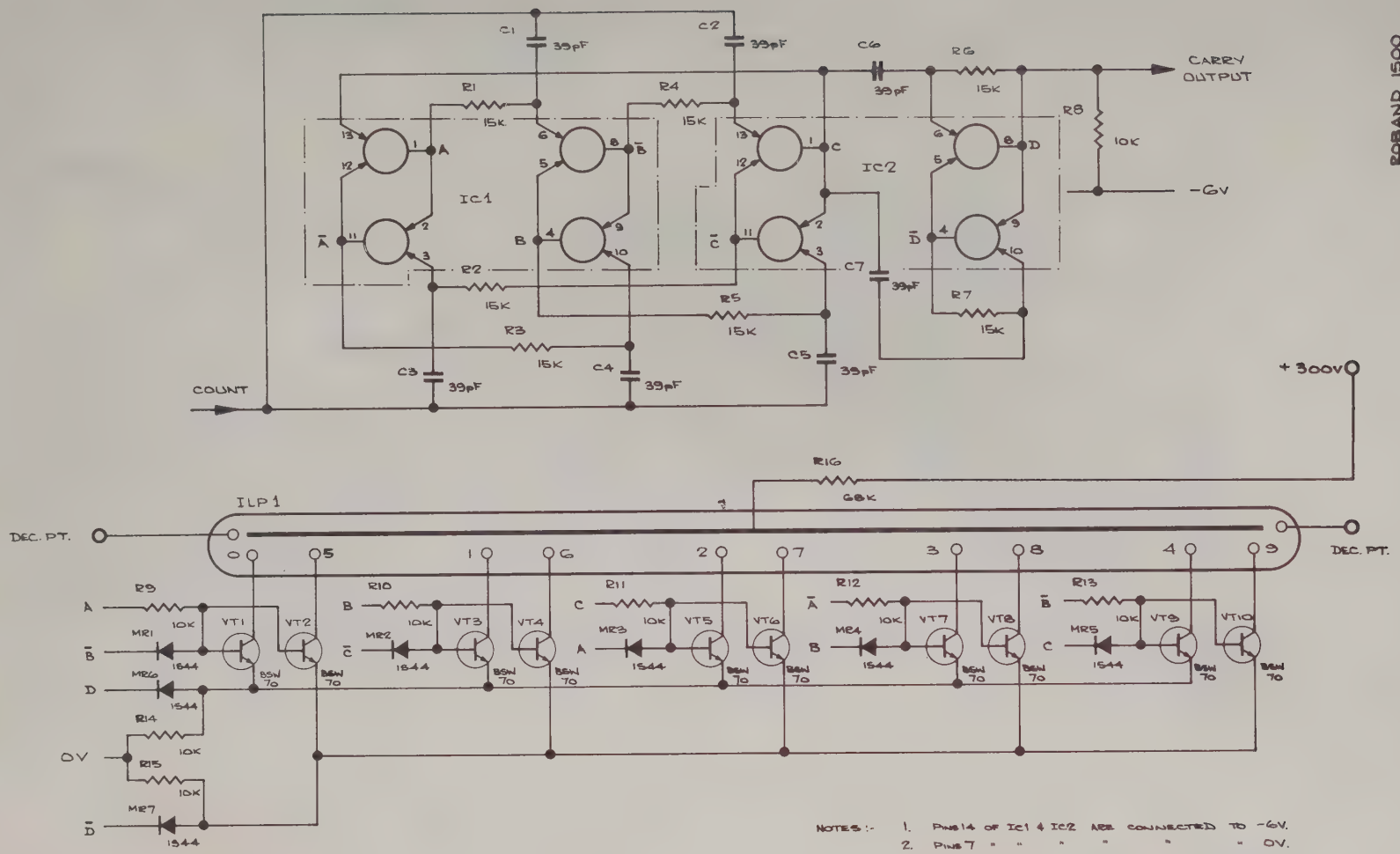



COUNTER WAVEFORMS FIG.8



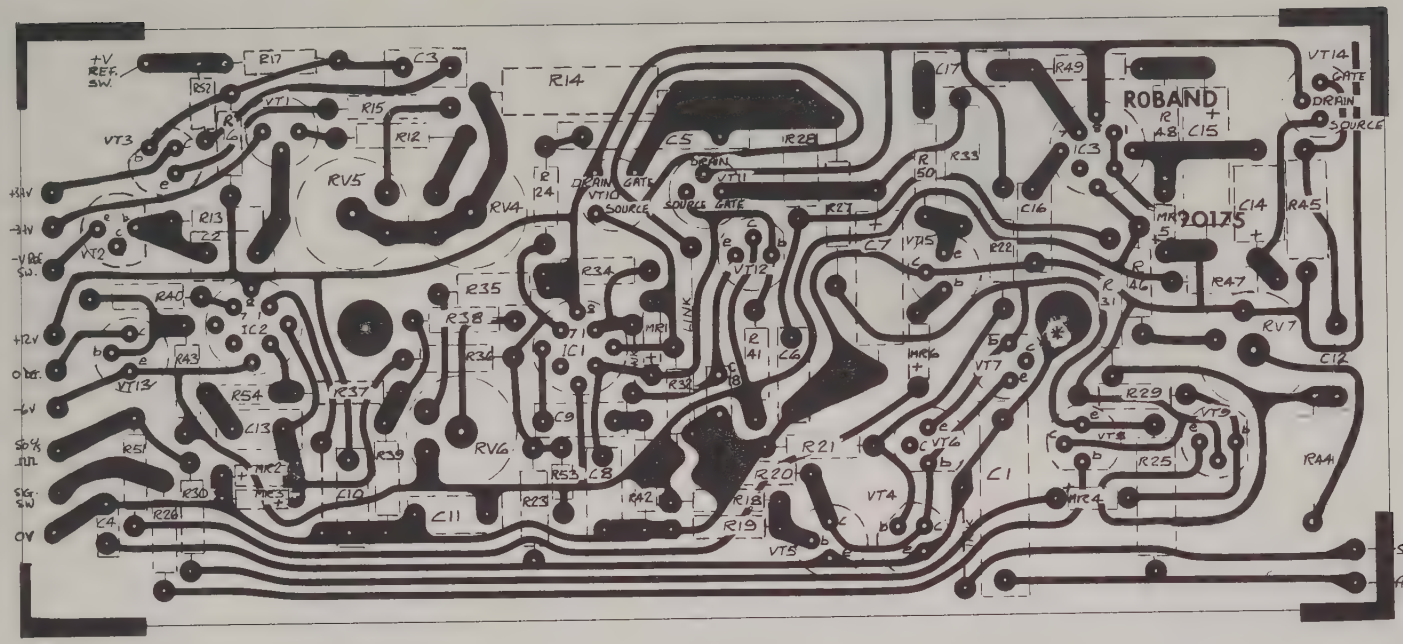

COUNTER ASSEMBLY 90176

FIG. 9



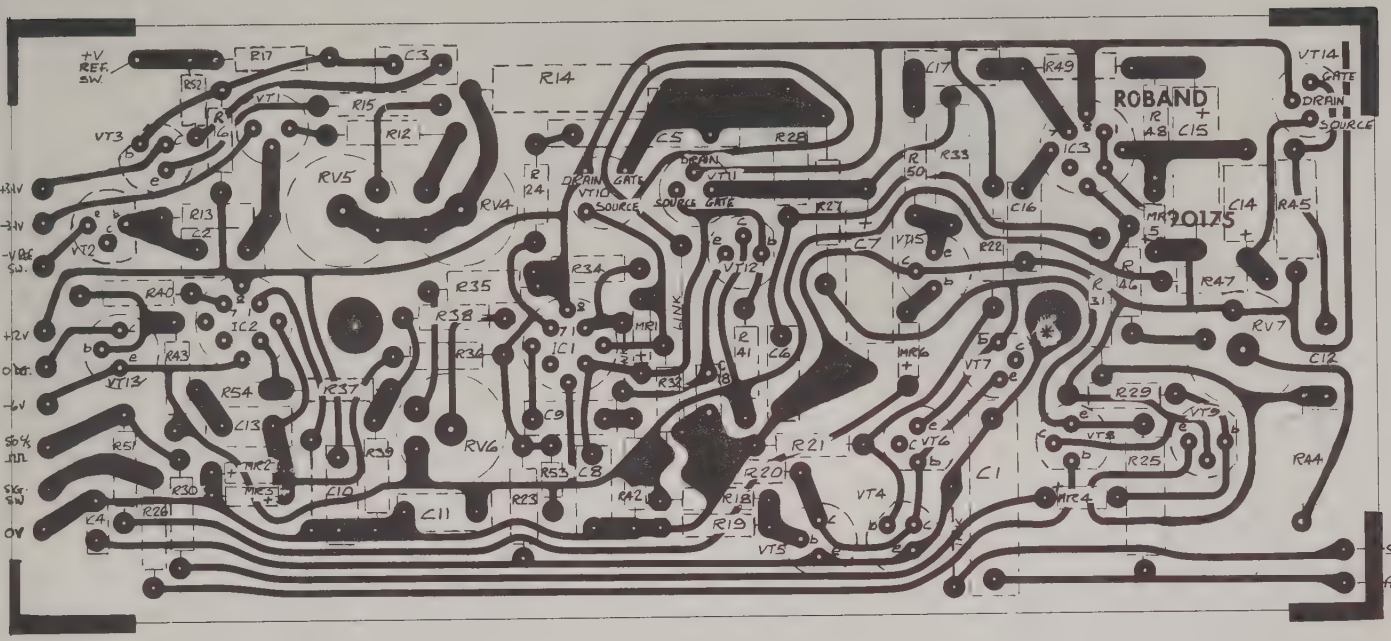

NOTES :-
1. PINS 14 OF IC1 & IC2 ARE CONNECTED TO -6V.
2. PINS 7 " " " " " " 0V.
3. L.H. DECIMAL POINT IS WIRED ON ALL BOARDS.
4. R.H. DECIMAL POINT IS WIRED ON UNITS BOARD ONLY.

COUNTER CCT. 901769 FIG.10



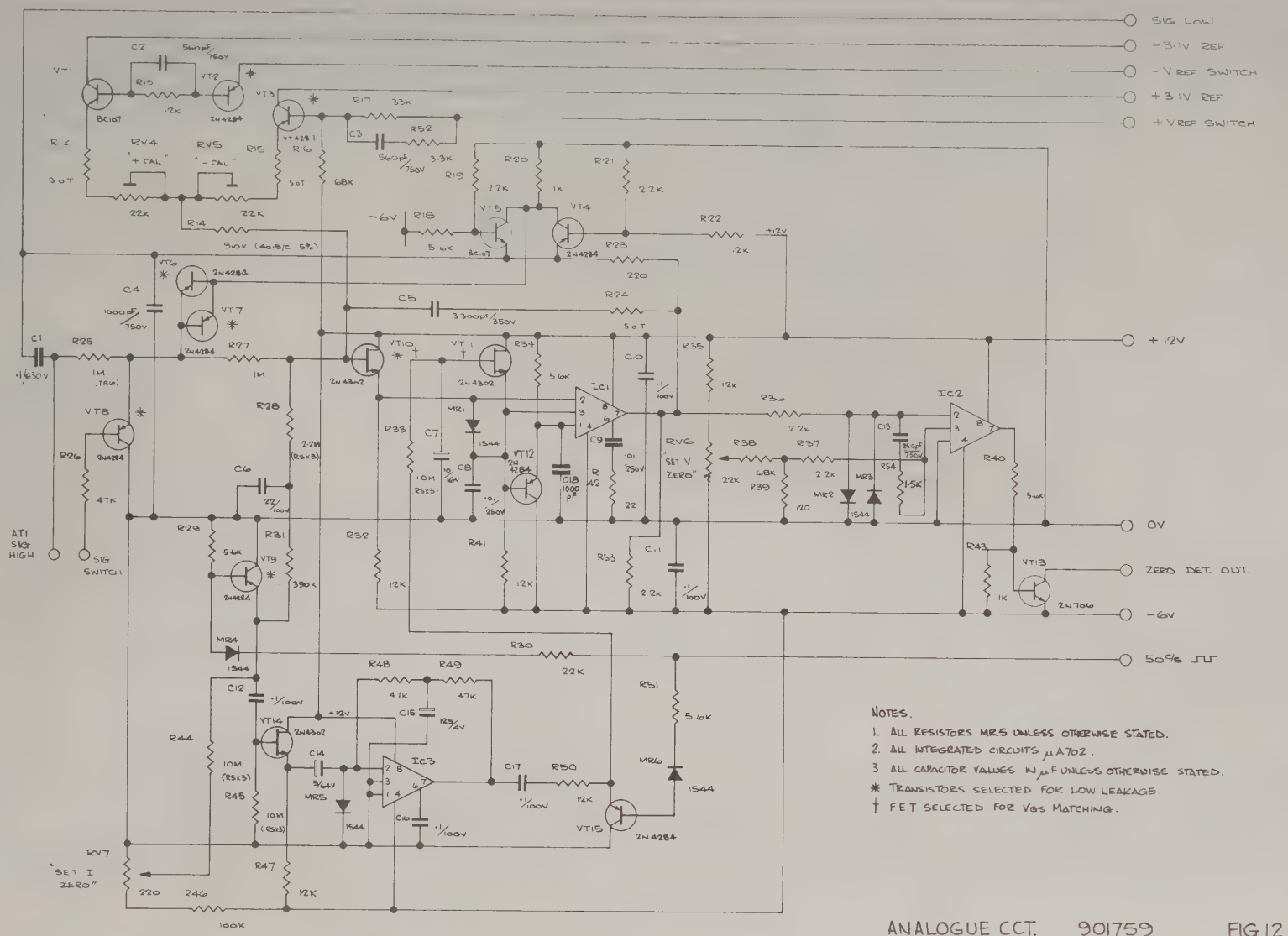

ANALOGUE ASSEMBLY 90175

FIG. 11




ANALOGUE ASSEMBLY 90175

FIG. 11




ROBAND 1500

NOTES.

1. ALL RESISTORS MR5 UNLESS OTHERWISE STATED.
2. ALL INTEGRATED CIRCUITS μA702.
3. ALL CAPACITOR VALUES IN μF UNLESS OTHERWISE STATED.

* TRANSISTORS SELECTED FOR LOW LEAKAGE.

† F.E.T SELECTED FOR $V_{GS}$ MATCHING.

ANALOGUE CCT. 901759 FIG.12

# WIRING SCHEDULE

## MAINS WIRING.

| | | | | |
|---|---|---|---|---|
| Mains Cable SW1.A. | SW1.A. Power Supply PCB (Transformer Primary Fuse) | Line Switched Line | Red<br>" | <br>14/0076 |
| Mains Cable SW1.B. | SW1.B. Power Supply PCB (Transformer Primary OV) | Neutral Switched Neutral | Black<br>" | <br>14/0076 |
| Mains Cable | Power Supply PCB (Earth). | Earth | Green | |

## POWER SUPPLY WIRING.

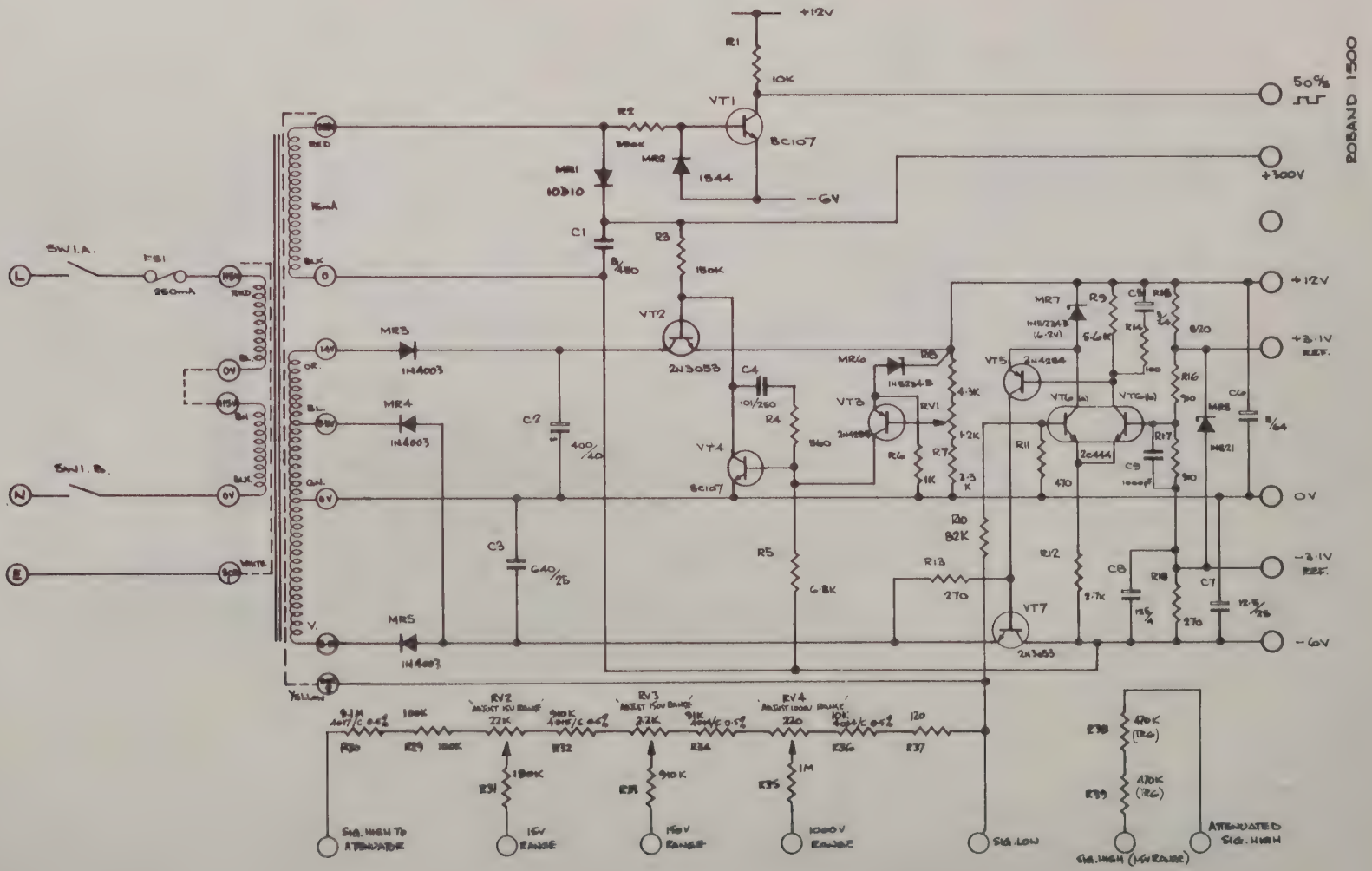
| | | | | |
|---|---|---|---|---|
| +300V (PS.PCB) | +300V (Units Counter). | +300V | Red | 14/0076 |
| +300V (Units Ctr.) | +300V (Tens Counter). | " | " | " |
| +300V (Tens Ctr.) | +300V (Hundreds Counter). | " | " | " |
| +300V (Hunds.Ctr.) | +300V (Control Logic). | " | " | " |
| –6V (PS.PCB) | –6V (Units Counter) | –6V | Blue | " |
| –6V (Units Ctr.) | –6V (Tens Counter) | " | " | " |
| –6V (Tens Ctr.) | –6V (Hundreds Counter) | " | " | " |
| –6V (Hunds.Ctr.) | –6V (Control Logic) | " | " | " |
| OV (PS.PCB) | OV (Units Counter) | OV | Black | " |
| OV (Units Ctr.) | OV (Tens Counter) | " | " | " |
| OV (Tens Ctr.) | OV (Hundreds Counter). | " | " | " |
| OV (Hunds.Ctr.) | OV (Control Logic) | " | " | " |
| OV (PS.PCB) | OV (Analogue PCB) | OV | Black | " |
| –6V (PS.PCB) | –6V (Analogue PCB) | –6V | Blue | " |
| +12V (PS.PCB) | +12V (Analogue PCB) | +12V | Orange | " |
| +3.1V (PS.PCB) | +3.1V (Analogue PCB) | +3.1V Ref. | Red/White | " |
| –3.1V (PS.PCB) | –3.1V (Analogue PCB) | –3.1V Ref. | Blk./White | " |
| 50c/s ⎍ (PS.PCB) | 50c/s ⎍ (Contr.Logic.PCB) | 50 c/s ⎍ | Pink | " |
| 50 c/s ⎍ (AN.PCB) | 50c/s ⎍ (Contr.Logic.PCB) | " ⎍ | " | " |

## RANGE SWITCH WIRING

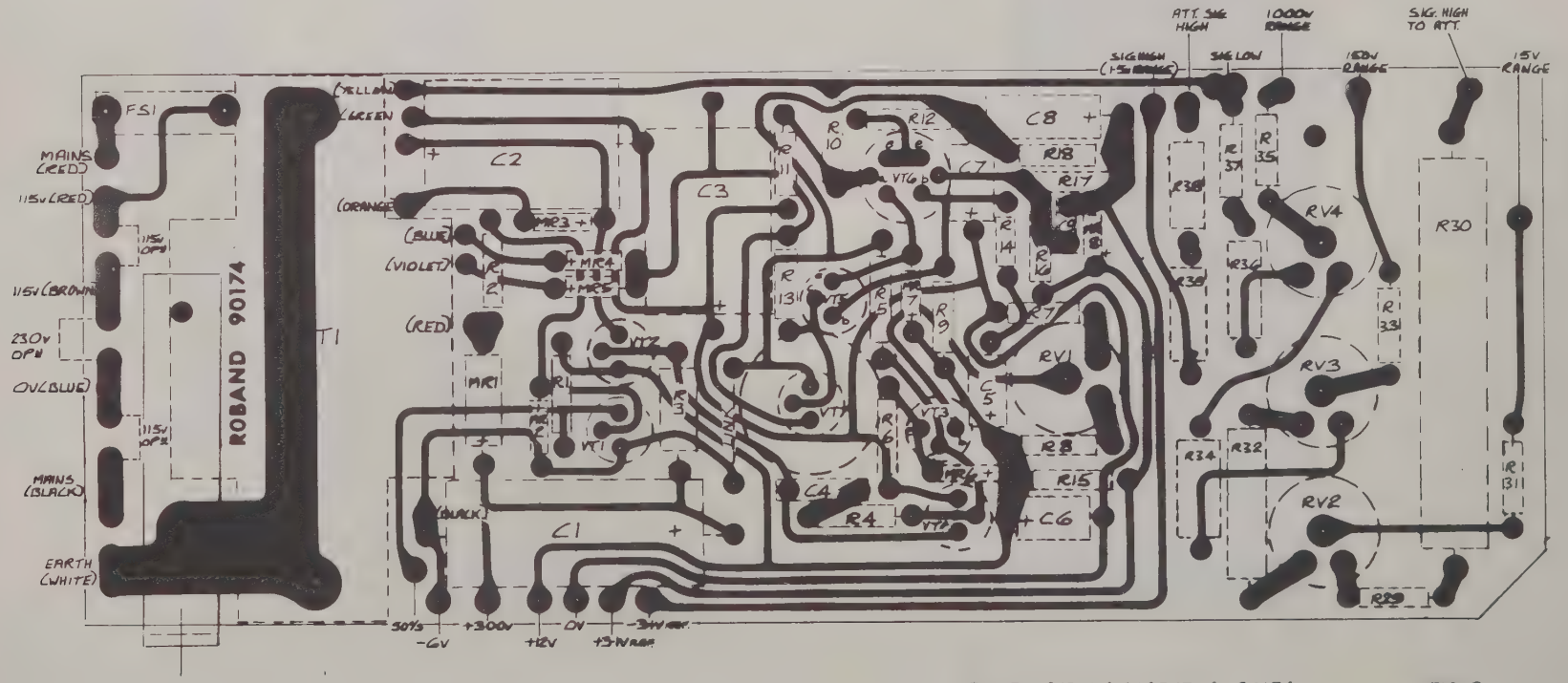
| | | | | |
|---|---|---|---|---|
| **WAFER 3** | | | | |
| Wiper | –6V (PS.PCB) | | Blue | 14/0076 |
| Posn 1 | Unit Counter Dec PT.R.H. | 1000v Dec PT. | White | " |
| Posn 2 | Unit Counter Dec PT. L.H. | 150v Dec PT. | Grey | " |
| Posn 3 | Ten Counter Dec PT. L.H. | 15v Dec PT. | Violet | " |
| Posn 4 | Hund. Counter Dec PT. L.H. | 1.5v Dec PT. | Yellow | " |
| **WAFER 2** | | | | |
| Sig. Low PS.PCB | Screen Tag | Sig. Low | Bn. | " |
| Screen Tag | Sig. Low (AN.PCB) | Sig. Low | Outer } | Screened PTFE |
| Wiper | Atten. Sig. High (AN.PCB) | Att. Sig. High | Inner } | Type CSSH 19/0076 |
| Wiper | Atten. Sig. High (PS.PCB) | Att.Sig. High | OR. | Type 3 |
| Posn 1 | 1000v Range (PS.PCB) | 1000v Range | White | " |
| Posn 2 | 150v Range (PS.PCB) | 150v Range | Grey | " |
| Posn 3 | 15v Range (PS.PCB) | 15v Range | Violet | " |
| **WAFER 1** | | | | |
| Wiper | Sig. High Input Term. (Red) | Sig. High | Inner } | Screened PTFE |
| Dummy Lug | Sig. Low Input Term. (Bk) | Sig Low | Outer } | Type CSSH 19/0076 |
| Dummy Lug | Front Screen | Sig. Low | Bn | 14/0076 |
| Dummy Lug | Sig. Low (PS.PCB) | Sig. Low | Bn | 14/0076 |
| Posn 1, 2, 3 | Sig. High to Att. (PS.PCB) | Sig. High to Att. | Red | Type 3 |
| Posn 4 | 1.5v Range (PS.PCB) | 1.5v Range | Yellow | " |

## INTERCONNECTIONS

| | | | | |
|---|---|---|---|---|
| Control Logic Count | Unit Counter Count | Count (Clock) | White/Green | 14/0076 |
| Unit Counter Carry | Tens Counter Count | Carry (5) | " | " |
| Tens Counter Carry | Hundreds Counter Count | Carry (50) | " | " |
| Hundreds Counter Carry | Control Logic 500 | Carry (500) | " | " |
| Control Logic +V Ref. SW. | Analogue PCB +Vref. SW. | +V Ref. Switch | Red/Blue | " |
| Control Logic –V Ref. SW. | Analogue PCB –V Ref. SW. | –V Ref. Switch | Blk/Blue | " |
| Control Logic Sig. Switch | Analogue PCB Sig. SW. | Signal Switch | White/Blue | " |
| Control Logic Zero Det. | Analogue PCB Zero Det. | Zero Detector | Red/Green | " |

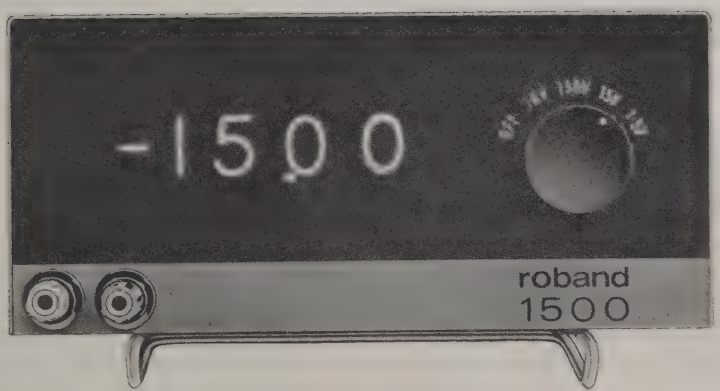



POWER SUPPLY CCT. 901749 FIG.3




POWER SUPPLY ASSEMBLY 90174 FIG. 2

# Reliability Report on the Roband 1500 Digital Voltmeter



**Summary**

A simple, general, picture is given of failure rate throughout life, showing a high early failure rate, falling to a lower rate which remains relatively steady, leading eventually to a rising failure rate as end of life approaches.

The customer is protected from the "early failures" by a period of soak test, and by the manufacturers guarantee.

An estimate of failure rate during the middle period is presented. While this cannot be regarded as an accurate figure, it gives an indication of the order of magnitude of failure rate.

Some implications of failure rate are considered. In particular, if the estimated failure rate of 9% per thousand hours is correct, an average of 9 failures per 100,000 unit hours could be expected. (Early failures and secondary failures are excluded). Corresponding probabilities of a given number of failures show a probability greater than .67 of not more than two failures in 22,000 hours, and probability greater than .95 of or not more than four failures in this time. The service life is estimated to be of the order of 50,000 hours, (dependant upon operating conditions), which is likely to be adequate. Some pointers are given to obtain maximum reliability by optimising working conditions.

**Variation of failure rate throughout life**

Fig. 1.

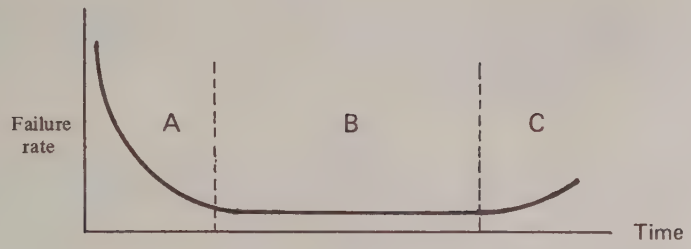



Fig. 1. shows a hypothetical relationship between failure rate, the number of failures per unit time, and time, for any electronic equipment.

Initially, A, failure rate is high, due to the inclusion of defective components which will fail prematurely, and to manufacturing defects in the equipment.

The failure rate falls to a lower and steady level, B. During this period, failures occur randomly. Eventually, C. the failure rate rises as components reach the end of their service life.

The purchaser of the equipment requires that the number of early failures be small, that the service life be long, and that the failure rate during service life should be low.

**Early failures**

Since the failure rate falls rapidly initially, the majority of early failures are detectable after a relatively short "soak test". A period of 200 hours is normally considered sufficient.

The equipment manufacturer will normally provide a guarantee for a limited period against faulty materials and workmanship.

**Other failures**

The "random failure" rate, and the service life, are considerably affected by operating conditions, notably by temperature and vibration.

Failures other than "random failures" also occur. These can be caused, for example, by accidental misuse of the equipment, or by secondary failures due to components being stressed during, or by incorrect repair of, a previous defect.

**Random Failure Rate**

Every equipment has an inherent failure rate, (dependant upon operating conditions) the difficulty is to determine it. Provided that, over a period of time, the failure rate does not vary with time, it is possible to make an assessment by accumulating the failures of a number of units over a period of time. Because of the random occurrence of defects, there is always a probability that the results are not truly representative, thus it is only possible to say, with a given degree of confidence, that failure rate is between given limits after a certain amount of testing, The test time necessary to establish tight limits to a high confidence level can be millions of unit hours.

**Failure Rate Estimates**

Alternatively, an estimate of failure rate can be obtained by considering the behaviour of the individual component parts of an equipment. Such an estimate cannot be used as a substitute for testing to give a guarantee of reliability. However, it can be used during the design stages of an equipment, to show where circuit or component changes may effect an improvement in reliability. In order to compile an estimate, the operating conditions of every component must be re-examined, in relation to its ratings. Subsequently a comparison of actual failures against the estimate can assist in design changes to further improve reliability.

A failure rate estimate can be used (with caution) to assess the repair requirements for a given number of units, to help to compile an economical spares requirement, and to calculate the probability of successful (or unsuccessful) operation during a given period. However, the accuracy of the estimate depends largely on the figures for part failure rates. Two equipments of comparable reliability can have widely different estimated failure rates, if part failure rate figures are obtained from different sources. To allow careful interpretation, a failure rate estimate must be presented with details of operating environment, relative component ratings, and the source of part failure rates.

Experience shows that estimates of failure rate are generally pessimistic, There are many reasons why this should be so. The component part failure rates are inevitably based on a limited amount of testing, and are thus likely to be pessimistic. Component failures include cases where one or more operating parameters move outside tolerance. In many cases, a circuit is so tolerant of these variations that performance is not degraded significantly.

It would be dangerous, however, to assume that failure rate is better than the estimated value, the estimate itself must be used with caution.

**Estimated Failure Rate of Roband 1500 (App.1, 2, 3).**

The estimated failure rate is 9% per thousand hours, assuming that operation is between 0-40°C,and in a laboratory environment. This implies an average of 9 failures per 100,000 unit hours. The estimated Mean Time between Failures (MTBF) is thus 11,000 hours. (It must be emphasised that this does not mean that a given unit will suffer 1 failure per 11,000 hours, such a failure pattern could not be described as random!).
In fact, the probability of a unit experiencing n failures in time t hours is given by

$$Pn = \frac{(\lambda t)^n}{n\ !} \quad e^{-\lambda t}$$

where $\lambda$ is the failure rate, estimated to be $9 \times 10^{-5}$. In particular, the probability of no failures in time t is

$$Po = e^{-\lambda t}$$

Thus the probability of successful operation for a given period may be estimated

As an example, the probabilities are given of various numbers of failures after 22,000 hours (11 years at 2,000 hours/yr), assuming a constant failure rate of $9 \times 10^{-5}$ for this time.

Po is approximately .135
P1 is approximately .271
P2 is approximately .271
P3 is approximately .180
P4 is approximately .090
P5 is approximately .036
P6 is approximately .012
P7 is approximately .003

A more practical idea of the degree of reliability may be obtained by comparison with the estimated failure rate, derived in the same way, of a commonly used unit. The Roband power supply unit type 67-5A is a high performance unit of proven reliability, with an estimated failure rate (APP4) of 2.7% per 1,000 hours. (37,000 hours MTBF). The ratio of estimated MTBFs is about 3½:1 the component ratio is about 7:1 (the voltmeter includes many integrated circuits), the ratio of soldered connections about 9:1. Such a comparison of unlike units is not truly valid, but does give an indication that the voltmeter is reliable for a unit of this complexity.

**Estimated Service Life**

The estimated service life of the electrolytic capacitors used is given as 75,000 hours.

The neon number tubes may give reduced brilliance by this time, particularly if certain cathodes are used for long periods of time.

The switch life will depend largely on the number of operations, but should normally give some tens of thousands of hours use. The service life is thus likely to be in the region of 30,000 to 50,000 hours.

**Conditions of use for maximum reliability**

The failure rate is reduced significantly by operation at temperatures close to 20°C. The ventilation slots, (base and rear) must not be blocked.

Failure rate is worsened by shock, vibration, corrosive atmosphere, high relative humidity.

Failure rate may be worsened by long periods of storage without use, particularly in hot or damp conditions. Operation for a 6-8 hour period every 3 months is recommended to reduce this deterioration.

Damage by improper use, other than mechanical damage is unlikely in normal operation. The unit will withstand 1,000 volts peak relative to earth (case) on either input terminal, and will not be damaged by applied signals of up to 1,000 volts on any range while operating. Damage could be caused by application of high signal voltages to the 1.5 volt range when no mains supply is connected. This may be prevented by switching the unit off using its combined range/on/off switch.

The mains supply must never exceed 20% above nominal. In particular, considerable damage could be caused by application of 230 volts mains to a unit connected for a 115 volt supply.

Care should be taken, when external connections are made to the voltmeter through the optional rear connector, to avoid short circuits between lines.

**APPENDIX 1 Estimated Failure rate. Roband 1500 digital voltmeter**

Component failure rates are taken from a chart published as a supplement to Electronic Components, September 1967, except where indicated*. Operation in a laboratory environment is assumed, at temperatures between 0-40°C.

| Quantity | Component | Relative Rating | Part failure rate | Total % 1000 hours |
|---|---|---|---|---|
| 69 | Resistors, Carbon composition | less than 1/10 rated power | .0075 | .5175. |
| 2 | " " " | " " ½ " " | .01125 | .0225. |
| 4 | " Carbon film | " " 1/10 " " | .075 | .3000 |
| 53 | " Metal Oxide Film | " " 1/10 " " | .003 | .1590 |
| 8 | " " " " | " " ½ " " | .0045 | .0360 |
| 9 | " Metal Film | " " 1/10 " " | .0075 | .0675 |
| 8 | Potentiometers Carbon Comp. | " " 1/10 " " | .05*APP3 | .4000 |
| 3 | Capacitors, Silvered Mica | less than 1/10 rated voltage | .045 | .1350 |
| 35 | " Ceramic | " " 1/10 " " | .015 | .5250 |
| 8 | " Plastic Film | " " 1/10 " " | .015 | .1200 |
| 8 | " Electrolytic A1. | " " | | |
| | Foil | " " ½ " " | )*APP2 | |
| 2 | " " " | " " rated voltage | ) | 3.3800 |
| 1 | " " Solid A1 | " " 1/10 " " | ) | |
| 3 | Diodes Silicon | less than ½ rated power | .01125 | .0338 |
| 30 | " " | " " 1/10 " " | .0075 | .2250 |
| 3 | " " Zener | " " 1/10 " " | .015 | .0450 |
| 1 | Transistor, Silicon | less than rated power | .024 | .0240 |
| 2 | " " | " " ½ " " | .018 | .0360 |
| 57 | " " | " " 1/10 " " | .012 | .6840 |
| 3 | Integrated Circuits, Linear T05 | | .045 | .1350 |
| 11 | " " digital plastic D.I.L. | | .03 | .3300 |
| 3 | Neon indicator diodes | | .03 | .0900 |
| 3 | Neon number indicator tubes | | .003* (Manufacturers figure). | .0090 |
| 14 | contacts Rotary switch | | .015 | .2100 |
| 6 | windings Power Transformer, impregnated | | .06 | .3600 |
| 1 | Fuse | | .03 | .0300 |
| 1000 | Soldered joints | | .001 | 1.0000 |
| | | | | 8.8843 |

Estimated failure rate is approximately 9% per thousand hours.

**APPENDIX 2 Capacitor Failure Rates**

The original estimate using the chart showed a very high failure rate attributed to electrolytic capacitors. An attempt has been made to improve this by reducing operating stresses, following the recommendations contained in the publication "MULLARD Electrolytic and Polyester Capacitors".

Thus the largest can size of a given capacitance value is used where possible. Operating voltage is below half the rated figure wherever possible, and never exceeds 0.7 of V max. The most significant factor affecting failure rate is temperature, the failure rate at 60°C is stated to be six times that at 40°C.

Unit operation to stated accuracy is specified to 40°C only. Operation up to 50°C. is permissible, with corresponding degredation of performance, reliability and life. Therefore, an ambient temperature of 40°C is assumed for this assessment.

Under these conditions, the following figures are given by the manufacturer.

| | | | | |
|---|---|---|---|---|
| 5. | C426 series, can sizes 2 and 3, | at or below ½ rated voltage | .18 | .90 |
| 1 | C426 series, can size 4 | " " ½ " " | .12 | .12 |
| 1 | C426 series, can size 4 | below rated voltage | .20 | .20 |
| 2 | C437 series, can size O3 | below ½ rated voltage | .13 | .26 |
| 1 | C415 solid al | | .10 | .10 |
| | | | | 1.58 |

There is one further high voltage capacitor for which no manufacturers figure is given. From the chart, the failure rate is given as .2 x 6 (operation above ½ rated voltage) x 1.5 (operation above 20°C) i.e. 1.8% per thousand hours.

Thus, the total failure rate for electrolytic capacitors is estimated to be 3.38% per thousand hours.

## APPENDIX 3

**Potentiometers and Variable resistors.**

The second largest contribution to failure rate, according to the original estimate, is made by 8 potentiometers and variable resistors. The following steps have been taken to minimise this contribution

1. The number of these components has been minimised, commensurate with ease of adjustment and calibration.

2. All potentiometers are greatly derated (the highest track dissipation is 6 milliwatts)

3. As far as possible, the associated circuits are such that relatively large variations of track resistance or contact resistance, will not significantly affect unit performance.

4. The types used, although not hermetically sealed, afford good protection against entry of dust and abrasive material.

5. Most important, the inherent circuit stability is such that the potentiometers rarely need adjustment. The customary front panel adjustments for zero and calibration, which could be used several times a day, are not required.

   Thus the actual failure rate of these components should be significantly reduced. An alternative figure of .05%/1000 hours is used.

## APPENDIX 4

Estimated failure rate of Roband Power Supply type 67-5A, operating at full load of 5A, and at 24V output, at 40°C, in a laboratory or workshop environment. Failure rate figures are as used in appendix 1.

| Quantity | Component | Relative Rating | Failure Rate | Total |
|---|---|---|---|---|
| 14 | Resistors metal oxide film | less than 1/10 rated power | .003 | .042 |
| 3 | " " " | less than ½ rated power | .005 | .015 |
| 2 | " wire wound power – | " " ½ " " | .0225 | .045 |
| 4 | Carbon potentiometers | " " 1/10," " | .05 | .200 |
| 3 | Transistors, silicon small signal | " " 1/10 " " | .012 | .036 |
| 1 | Transistors , silicon power driver | " " ½ " " | .180 | .180 |
| 2 | Transistors silicon, power output | " " ½ " " | .180 | .360 |
| 4 | Diodes (Rectifier bridge) | less than rated power | .150 | .600 |
| 2 | Diodes silicon zener | " " 1/10 " " | .015 | .030 |
| 1 | " " " | " " ½ " "" | .023 | .023 |
| 1 | Capacitor, plastic film | less than 1/10 rated voltage | .015 | .015 |
| 1 | " " " | less than ½ " " | .045 | .045 |
| 1 | Transformer 10 windings | | .060 | .600 |
| 1 | Fuse | | .020 | .020 |
| 1 | Capacitor type C437 | less than ½ rated voltage | .130 | .130 |
| 1 | Capacitor (reservoir) long life | approx. ½ rated voltage. | .250 | .250 |
| 110 | Soldered joints | | .001 | .110 |
| | | | | 2.701 |

Estimated failure rate 2.7% per thousand Hours.
Estimated Mean Time between Failures 37,000 hours.

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